TECHNISCHE DOCUMENTATIE 1969
DEEL 9 — SEPTEMBER

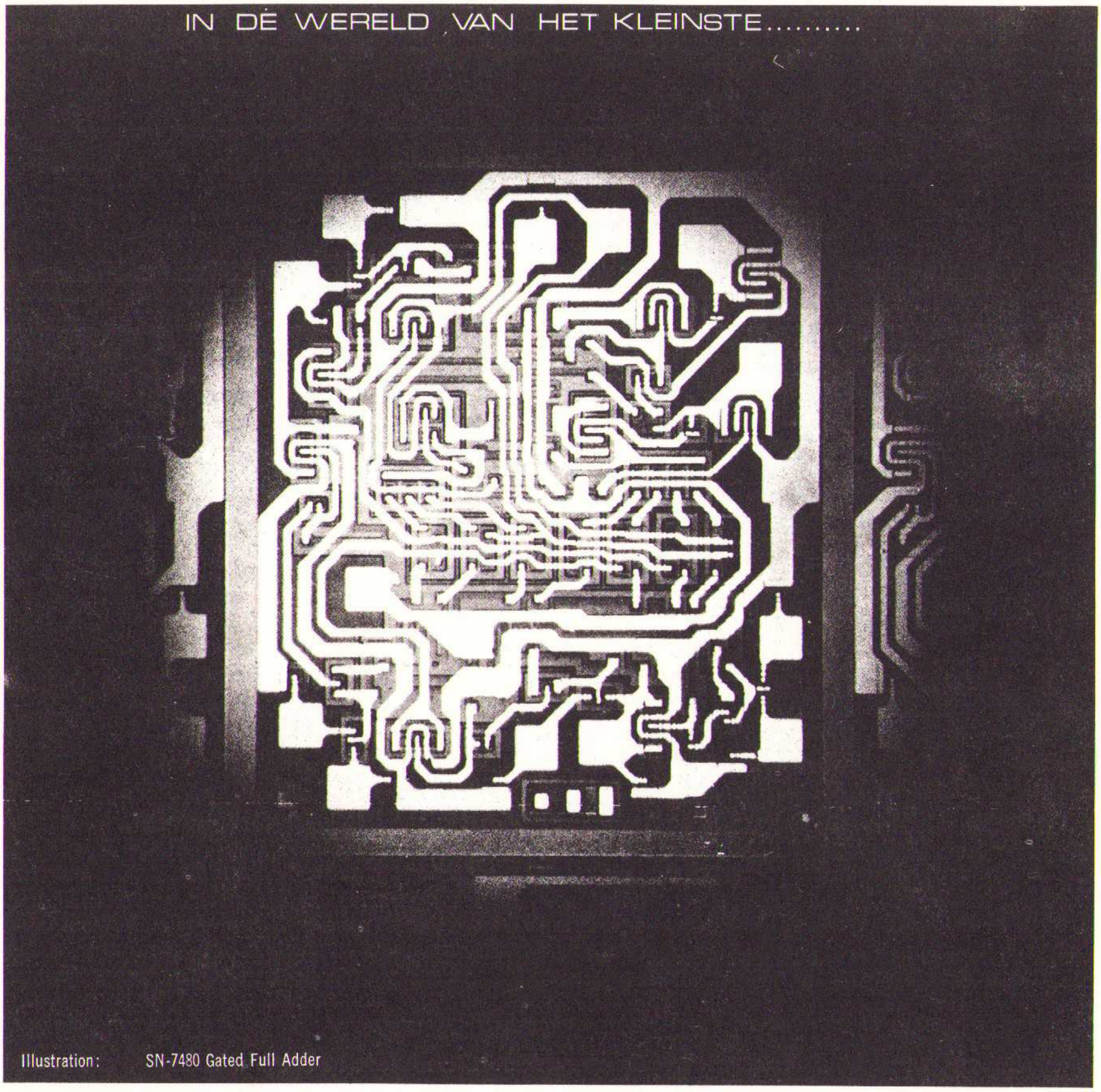

Illustration: SN-7480 Gated Full Adder

PRIJS ƒ 1,50

Technische documentatie 1969, tweede jaargang, september 1969

Abonnementsprijs per jaar *f* 10,40 incl. 4% B.T.W.

Omslagfoto: geïntegreerde schakeling, schijfje silicium met een complete versterker, ware grootte circa 1 mm^2.

Verhuizingen:
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Inleiding bij deel 9.

In deze nieuwe uitgave wordt weer in ruime mate aandacht besteed aan verscheidene interessante produkten door middel van het opnemen van de volledige datasheets en de bij het produkt behorende toepassingen. Met opzet hebben wij alle gegevens en de tekst in de oorspronkelijke taal laten staan, teneinde te voorkomen, dat de (technische) bedoelingen door vertaling verdoezeld worden.

Tevens is aan ons zo bekende programma van digitale bouwstenen een nieuwe uitvoering toegevoegd, welke geheel uitwisselbaar is met de teller met het uit discrete componenten opgebouwde geheugen; door het op de markt komen van een geïntegreerd RTL-geheugen is het aantal soldeerpunten drastisch beperkt.

★ TOT SLOT WIJZEN WIJ U ER MET GROTE NADRUK OP, DAT ZOWEL UW CORRESPONDENTIE ALS UW POSTORDERS DIENEN TE WORDEN GESTUURD AAN ONS POSTBUS - ADRES:

Van Dam Elektronica, Postbus 3149 te Rotterdam-noord*

DIT VOORKOMT ONNODIGE VERTRAGING IN DE BEHANDELING TEN GEVOLGE VAN DE EEN MAAL PER DAG PLAATSHEBBENDE POSTBESTELLING !!!!!!!!

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GALVANOMETER AMPLIFIER

Galvanometers are the most common instruments used to detect the balance point of D.C. bridges. The sensitivity of the galvanometer is one of the principal factors which determine the accuracy with which the balance point can be obtained. The circuit (Fig. 4.4.1) described in this Section in an amplifier which can be used to increase the sensitivity of a galvanometer by a factor of up to 50, allowing a corresponding increase in bridge sensitivity to be obtained.

The circuit is a conventional long-tailed-pair using the dual low-level, low-noise transistor 2C 415 and is designed to be operated from a floating battery supply of 4.5 to 6 volts. With the switch S_1 in position 1 the battery is disconnected from the circuit and the galvanometer G is connected directly to the input terminals. With the switch in position 2 the battery is connected and the current to be measured generates a voltage which is amplified and displayed on the galvanometer.

Before using the amplifier null is adjusted by making the contact S_2, which should be a spring loaded switch, setting S_1 to position 2 and adjusting P_1 for a null indication on the galvanometer. Similarly the balance potentiometer P_2 is adjusted with the contact S_2 open, the circuit inputs open and a null reading on the galvanometer is obtained.

At the start of any measurement the sensitivity control P_3 should be set for minimum resistance to give minimum sensitivity. As balance is obtained the sensitivity can be increased by increasing the resistance in P_3.

NOTES

1. It will normally be most convenient to use this circuit with a battery supply. If a power unit is used it must be floating with respect to the input terminals.
2. The resistors marked with an asterisk should be 1% high stability types (such as Erie Type MOG 60). All other resistors are Erie Type 16 or other similar 1/2 watt types with 10% tolerance.
3. Suitable potentiometers are Painton Bourn Trimpots Type 200.

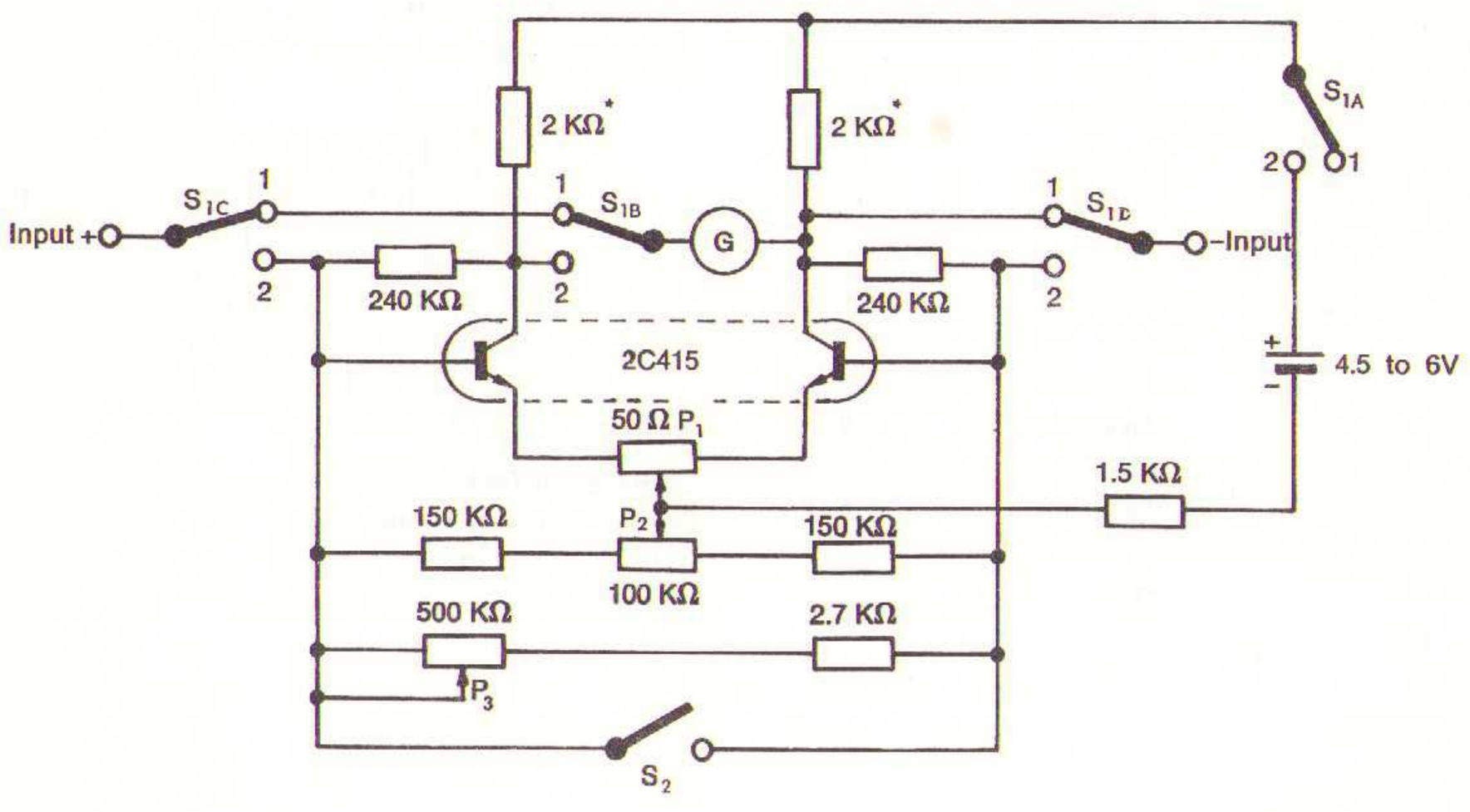


Fig. 4.4.1 - Galvanometer Amplifier

Literatuur: Technische documentatie 1969 deel 7-8 (blz. 3-5): datasheets.
SGS-FAIRCHILD: industrial circuit handbook.

TAB101

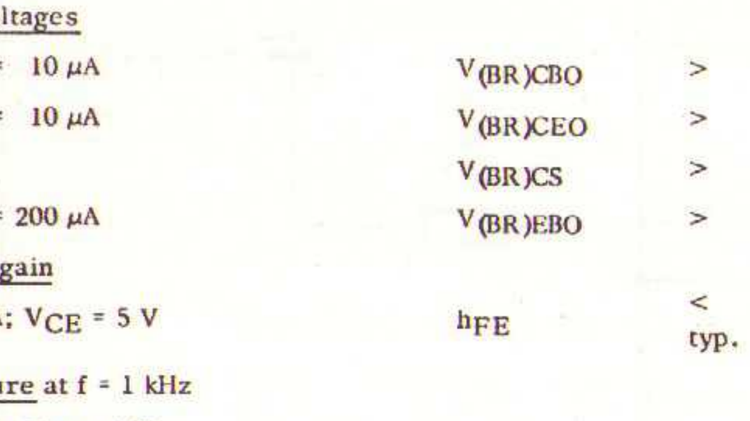
RING (DE)MODULATOR FOR TELEPHONY AND INDUSTRIAL EQUIPMENT

The TAB101 is a monolithic integrated circuit comprising a 4-transistor modulator and demodulator circuit. The circuit being made on a single crystal ensures a great similarity in characteristics of the transistors and optimal tracking of their parameters with temperature variations. Consequently, the TAB101 gives a better balancing and therefore less carrier leakage than a conventional circuit. The use of transistors instead of diodes provides a better isolation between input and output circuits.

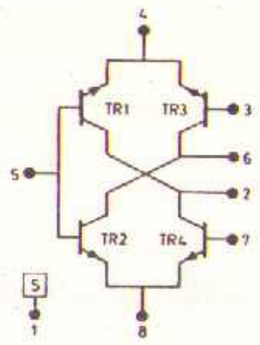
QUICK REFERENCE DATA				
Collector cut-off current V_{CB} = 5 V; T_{amb} = 25 °C	I_{CBO}	<	100	nA
Base-emitter voltage differences between transistors 1, 2, 3, 4 V_{CB} = 5 V; $-I_E$ = 150 μA	$\lvert V_{BE1}-V_{BE2}\rvert$	<	5	mV
	$\lvert V_{BE3}-V_{BE4}\rvert$	<	5	mV
Common-base current gain differences between transistors 1, 2, 3, 4 V_{CB} = 5 V; $-I_E$ = 150 μA	$\lvert h_{FB1}-h_{FB2}\rvert$	<	0.008	
	$\lvert h_{FB3}-h_{FB4}\rvert$	<	0.008	

PACKAGE OUTLINE Dimensions in mm

XA10; TO-74 (reduced height)



CIRCUIT DIAGRAM



RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

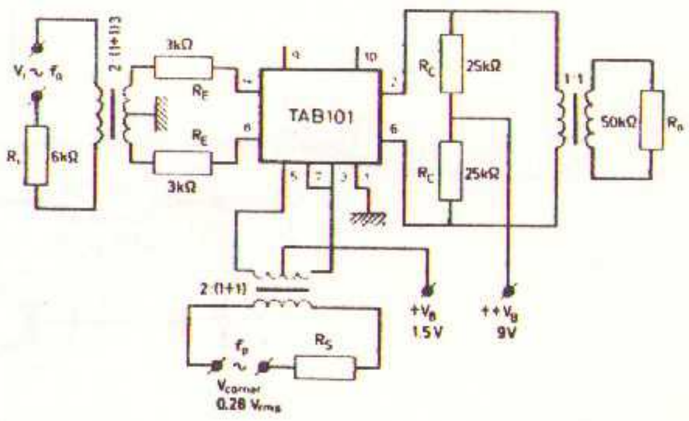
Voltages (each transistor)				
Collector-base voltage (open emitter)	V_{CBO}	max.	10	V
Emitter-base voltage (open collector)	V_{EBO}	max.	5	V
Collector-substrate voltage	V_{CS}	max.	12	V
Currents (each transistor)				
Collector current	I_C	max.	10	mA
Power dissipation (4 transistors)				
Total power dissipation up to T_{amb} = 100 °C	P_{tot}	max.	100	mW
Temperatures				
Storage temperature	T_{stg}		−35 to +125	°C
Operating ambient temperature	T_{amb}		−25 to +100	°C

CHARACTERISTICS (each transistor)

			T_{amb} = 25 °C	
Collector cut-off current				
I_E = 0; V_{CB} = 5 V	I_{CBO}	typ.	5	nA
		<	100	nA
Collector-substrate leakage current				
V_{CS} = 9.5 V	I_{CS}	typ.	5	nA
		<	100	nA
Emitter cut-off current				
I_C = 0; V_{EB} = 1 V	I_{EBO}	typ.	5	nA
		<	100	nA
Break down voltages				
I_E = 0; I_C = 10 μA	$V_{(BR)CBO}$	>	10	V
I_B = 0; I_C = 10 μA	$V_{(BR)CEO}$	>	9	V
$-I_S$ = 10 μA	$V_{(BR)CS}$	>	12	V
I_C = 0; I_E = 200 μA	$V_{(BR)EBO}$	>	5	V
D.C. current gain				
I_C = 150 μA; V_{CE} = 5 V	h_{FE}	<	20	
		typ.	75	
Spot noise figure at f = 1 kHz				
$-I_E$ = 150 μA; V_{CB} = 5 V				
R_S = 1 kΩ; Bandwidth: 200 Hz		typ.	6	dB
Base-emitter voltage difference				
between transistors TR1 and TR2 at				
$-I_{E1} = -I_{E2}$ = 150 μA; $V_{CB1} = V_{CB2}$ = 5 V	$\lvert V_{BE1}-V_{BE2}\rvert$	typ.	2	mV
		<	5	mV
between transistors TR3 and TR4 at				
$-I_{E3} = -I_{E4}$ = 150 μA; $V_{CB3} = V_{CB4}$ = 5 V	$\lvert V_{BE3}-V_{BE4}\rvert$	typ.	2	mV
		<	5	mV
Current amplification factor difference				
between transistors TR1 and TR2 at				
$-I_{E1} = -I_{E2}$ = 150 μA; $V_{CB1} = V_{CB2}$ = 5 V	$\lvert h_{FB1}-h_{FB2}\rvert$	typ.	0.002	
		<	0.008	
between transistors TR3 and TR4 at				
$-I_{E3} = -I_{E4}$ = 150 μA; $V_{CB3} = V_{CB4}$ = 5 V	$\lvert h_{FB3}-h_{FB4}\rvert$	typ.	0.002	
		<	0.008	

APPLICATION INFORMATION

Telephony carriers ring modulator



Performance at T_{amb} = 25 °C

Conversion gain at f_a = 1 kHz, V_i = 0.4 V; f_p = 34 kHz	G_c	typ.	−0.75	dB
Carrier leakage power in R_o at f_p = 34 kHz	P_{oc}	typ.	3	nW

TAA 263

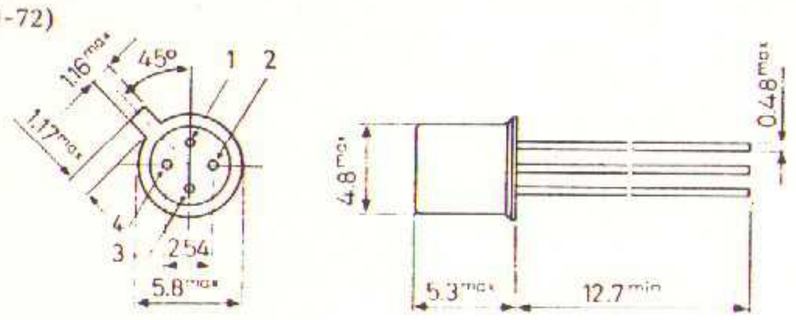
LOW-LEVEL AMPLIFIER

The TAA263 is a semiconductor integrated amplifier in a 4-lead TO-72 metal envelope. It comprises a three-stage, direct coupled low-level amplifier for use from d.c. up to frequencies of 600 kHz.

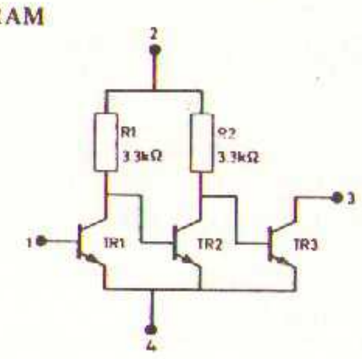
QUICK REFERENCE DATA				
Supply voltage	V_B	max.	8	V
Output voltage	V_{3-4}	max.	7	V
Output current	I_3	max.	25	mA
Transducer gain at P_o = 10 mW				
R_L = 150 Ω; f = 1 kHz	G_{tr}	typ.	77	dB
Operating ambient temperature	T_{amb}	−20 to +100		°C

PACKAGE OUTLINE Dimensions in mm

XC4 (TO-72)

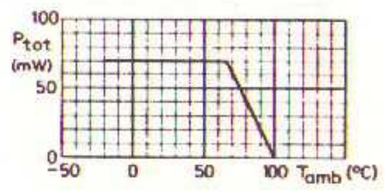


CIRCUIT DIAGRAM



RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

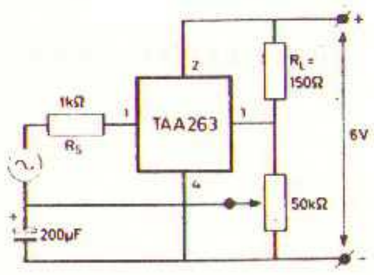
Voltages				
Supply voltage	V_B	max.	8	V
Output voltage	V_{3-4}	max.	7	V
Input voltage	$-V_{1-4}$	max.	5	V
Currents				
Output current	I_3	max.	25	mA
Input current	I_1	max.	10	mA
Power dissipation				
Total power dissipation up to T_{amb} = 65 °C	P_{tot}	max.	70	mW



Temperatures				
Storage temperature	T_{stg}	−65 to +100		°C
Operating ambient temperature	T_{amb}	−20 to +100		°C

CHARACTERISTICS T_{amb} = 25 °C

Test circuit:



Currents				
Output current	I_3	typ.	12	mA
Total current drain (no signal)	I_2+I_3	<	16	mA
Over-all small signal current gain				
f = 1 kHz	$h_{f\,tot}$	typ.	5.10^5	
Transducer gain				
f = 1 kHz; P_o = 10 mW	G_{tr}	>	70	dB
		typ.	77	dB
Output power at f = 1 kHz; d_{tot} = 10%	P_o	>	10	mW
d_{tot} = 5%	P_o	>	8	mW
Noise figure				
f = 400 Hz to 6 kHz	F	typ.	5	dB
		<	10	dB
f = 450 kHz; Δf = 5 kHz	F	typ.	2.7	dB

CHARACTERISTICS (continued) T_{amb} = 25 °C

y parameters (point 4 common connection)

V_B = 6 V; I_3 = 3 mA; V_{3-4} = 4.2 V

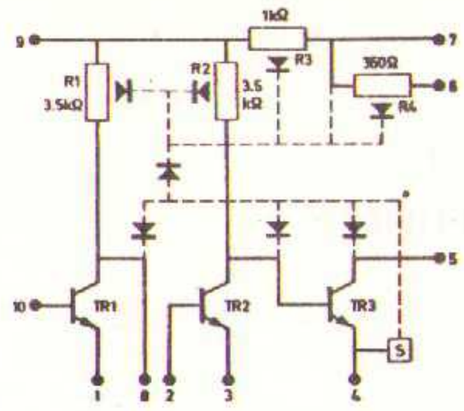
f = 1 kHz				
Input admittance	$y_i = g_i$	typ.	20	$\mu\Omega^{-1}$
Transfer admittance	$y_f = g_f$	typ.	11	Ω^{-1}
Output admittance	$y_o = g_o$	typ.	60	$\mu\Omega^{-1}$
f = 450 kHz				
Input conductance	g_i	typ.	15	$\mu\Omega^{-1}$
Input capacitance	C_i	typ.	14	pF
Transfer admittance	$\|y_f\|$	typ.	9.4	Ω^{-1}
Phase angle of transfer admittance	φ_f	typ.	125°	
Output conductance	g_o	typ.	20	$\mu\Omega^{-1}$
Output capacitance	C_o	typ.	13	pF

TAA293
GENERAL PURPOSE AMPLIFIER

The TAA293 is a general purpose integrated amplifier which can be applied in various audio and i.f. applications. Its configuration furthermore allows the use of the TAA293 in multivibrators, pulse amplifiers, trigger circuits, etc.

QUICK REFERENCE DATA				
Supply voltage	V_B	nom.	+6.0	V
Small signal current gain of first transistor I_8 = 1 mA; V_{8-1} = 1 V	h_{fe}	typ.	80	
Transducer gain	G_{tr}	typ.	80	dB
Noise figure (30 to 15000 Hz)	F	typ.	6	dB
Frequency response (−3 dB)		typ.	600	kHz

CIRCUIT DIAGRAM

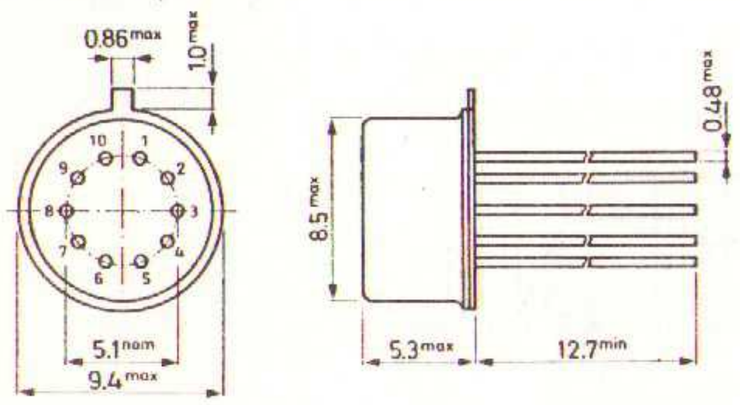


Note:

The diodes drawn with dotted lines are the parasitic diodes formed by the P-N junction of the resistor-diffusions in the N-isle and of the N-isle to the P-substrate respectively. Taking account of the parasitic diodes one can prevent any unwanted effects due to their becoming conducting under certain conditions of d.c. potentials or signal voltages.

PACKAGE OUTLINE Dimensions in mm

XA10 (TO-74; reduced height)



RATINGS Limiting values in Accordance with the Absolute Maximum System (IEC134)

Voltages

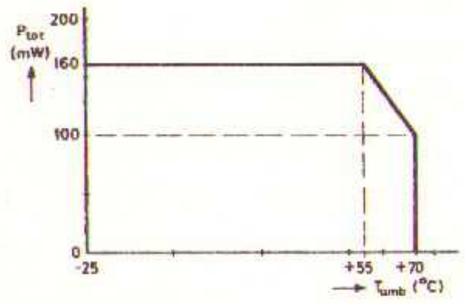
V_{9-1}	max.	7.0	V
V_{8-1}	max.	7.0	V
V_{8-10}	max.	7.0	V
V_{9-3}	max.	7.0	V
V_{9-4}	max.	7.0	V
V_{8-4}	max.	7.0	V
V_{7-4}	max.	7.0	V
V_{6-4}	max.	7.0	V
V_{5-4}	max.	7.0	V
V_{1-10}	max.	6.0	V
V_{3-2}	max.	6.0	V

Currents

I_5	max.	40	mA
$-I_4$	max.	40	mA
$-I_1$	max.	20	mA
I_8	max.	20	mA
$-I_3$	max.	10	mA
I_{10}	max.	10	mA
I_2	max.	10	mA

RATINGS (continued)

Total power dissipation



Temperatures

Storage temperature	T_{stg}		−25 to +100	°C
Operating ambient temperature	T_{amb}	max.	70	°C

CHARACTERISTICS at T_{amb} = 25 °C

Small signal current gain

of first transistor I_8 = 1 mA; V_{8-1} = 1 V	h_{fe}	>	30	
		typ.	80	

Saturation voltage

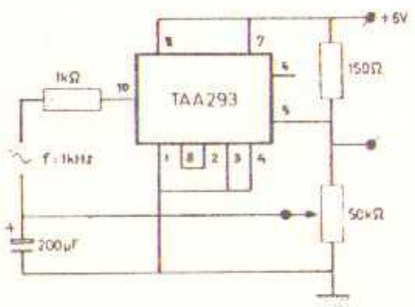
of last transistor at I_5 = 24 mA	$V_{5-4\ sat}$	<	2	V

Noise figure

$-I_1$ = 100 μA; R_S = 2 kΩ	F	typ.	6	dB
B = 30 Hz to 15000 Hz		<	10	dB

Transducer gain	G_{tr}	typ.	80	dB
Output power at d_{tot} = 10%	P_o	>	10	mW

Test circuit for measuring the transducer gain and the output power



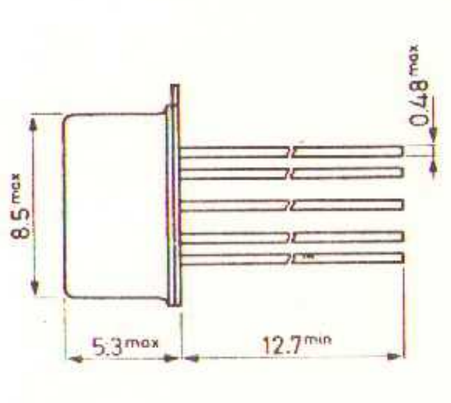
TAA310
A.F. PREAMPLIFIER

The TAA310 is a monolithic integrated circuit designed for use as an a.f. high-gain preamplifier, with a very low noise figure (< 4 dB) and a high voltage gain of at least 90 dB. Because this gain can be achieved at a low load impedance (1 kΩ) and the input impedance is high, the TAA310 is specially suited for the recording and playback amplifier in tape recorders.

QUICK REFERENCE DATA				
Supply voltage	V_B	nom.	+7	V
Voltage gain	G_v	typ.	100	dB
Noise figure	F	≤	4	dB
Input impedance	z_i	typ.	20	kΩ

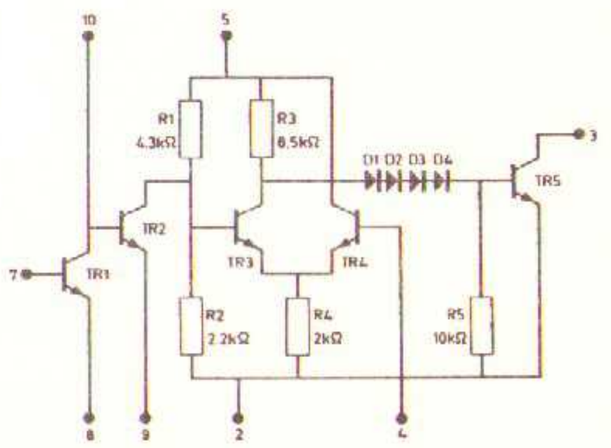
PACKAGE OUTLINE Dimensions in mm

XA10 (TO-74; reduced height)



Pins 1 and 6 are not connected

CIRCUIT DIAGRAM



RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

Voltages

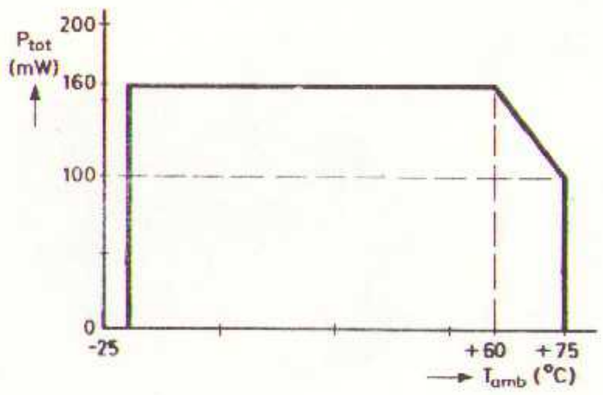
V_{5-2}	max.	9.5	V
V_{3-2}	max.	9.5	V
V_{10-8}	max.	6	V
V_{8-7}	max.	6	V
V_{9-10}	max.	6	V
V_{4-2}	max.	6	V

The pins 3, 4, 5 and 10 must never have a negative potential with respect to pin 2 (substrate).

Currents

I_3	max.	20	mA
I_7	max.	3	mA
$-I_8$	max.	10	mA
$-I_9$	max.	10	mA
I_{10}	max.	10	mA
I_4	max.	3	mA

Total power dissipation



Temperatures

Storage temperature	T_{stg}	−20 to +80	°C
Operating ambient temperature	T_{amb}	−20 to +75	°C

[1]) Limiting values according to the Absolute Maximum System as defined in IEC publication 134.

CHARACTERISTICS at T_{amb} = 25 °C

D.C. current gain

of first transistor
I_{10} = 100 μA; V_{10-7} = 0 — h_{FE} > 40

Input impedance at f = 1 kHz

I_{10} = 100 μA; V_{10-7} = 0 — z_i typ. 20 kΩ

Saturation voltage

of output transistor at I_3 = 7 mA — $V_{3-2\ sat}$ typ. 0.8 V; < 1.2 V

Voltage gain — G_v > 93 dB

Noise figure

R_S = 2 kΩ; B = 30 to 15 000 Hz — F typ. 2.5 dB; < 4 dB

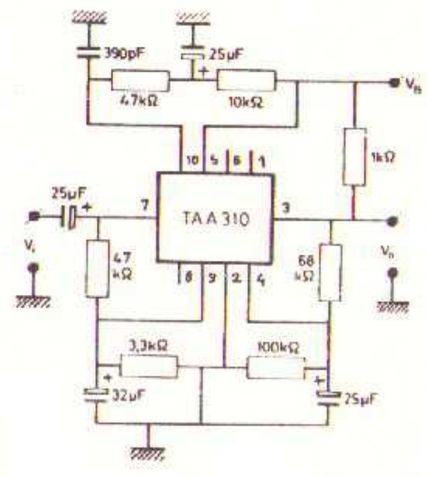
Output voltage at d_{tot} = 10% — $V_{o(rms)}$ typ. 2 V

Cut-off frequency (−3 dB) — f_c ≥ 15 kHz

D.C. collector voltage

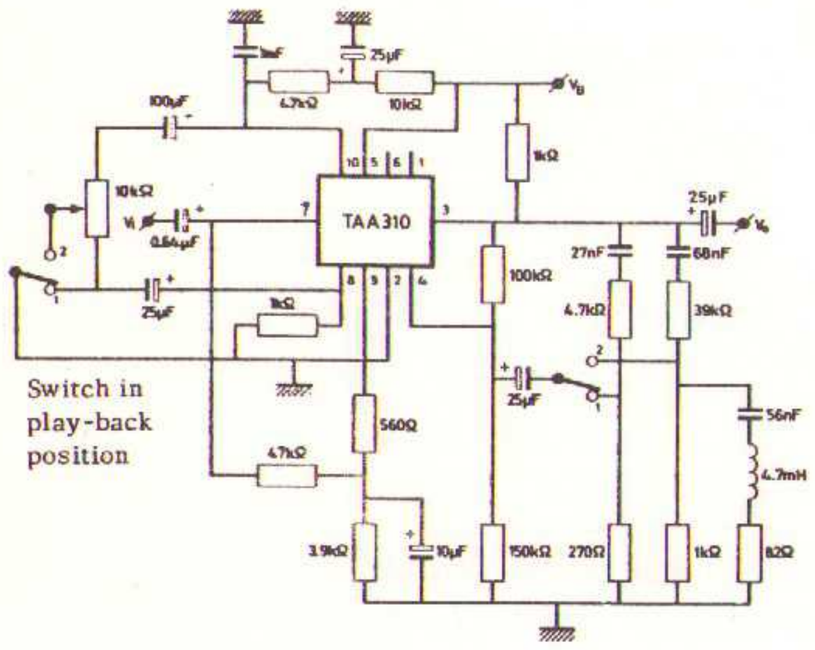
of output transistor at I_9 = 200 μA — V_{3-2} typ. 3.8 V; 3.4 to 4.2 V

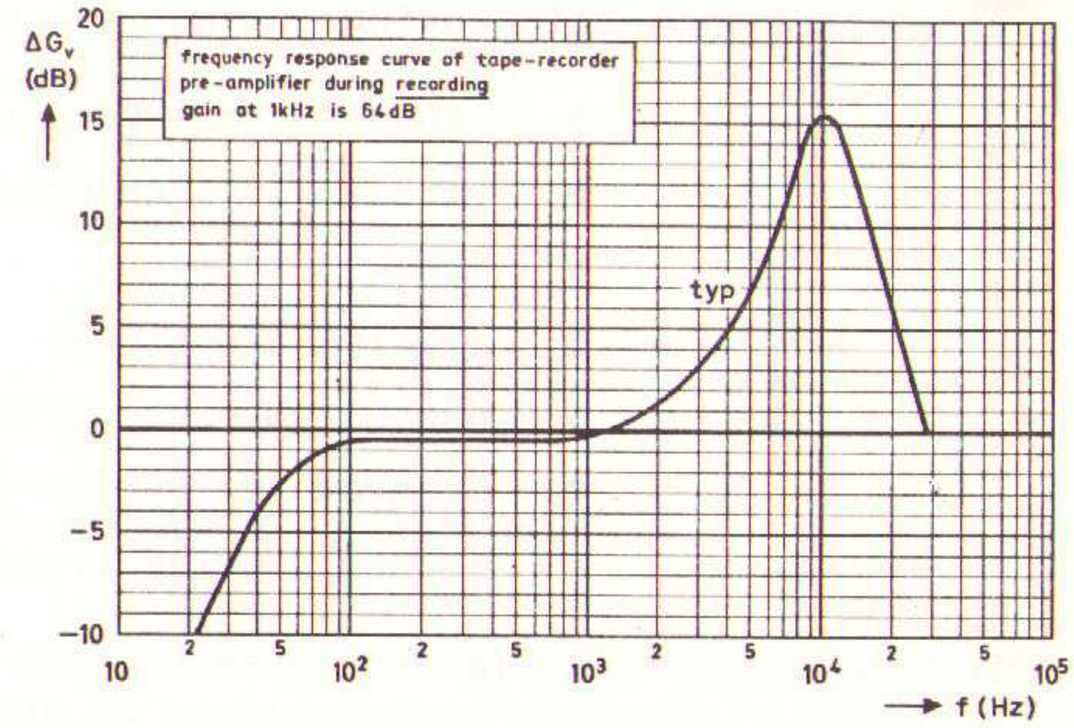
Test circuit for measuring G_v, F, $V_{o(rms)}$, f_c and V_{3-2} at V_B = 7 V ←



APPLICATION INFORMATION

Practical tape-recorder preamplifier with a TAA310.



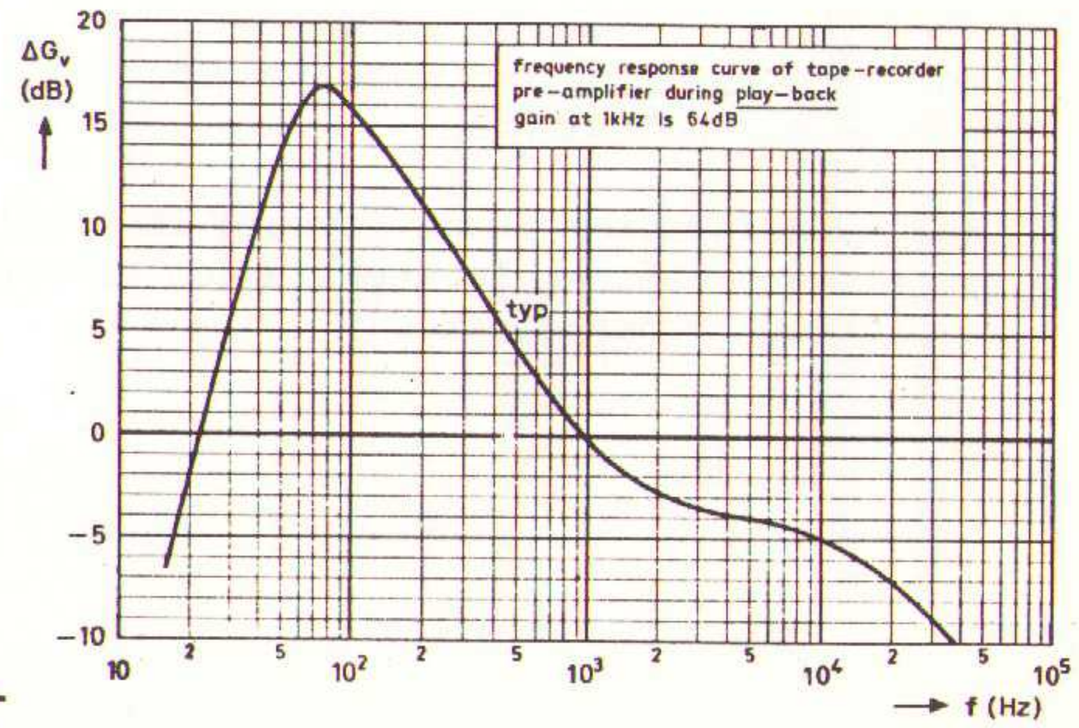


Data for use as recording amplifier (measured at f = 1 kHz)

Voltage gain	G_v		64 ± 2	dB
Frequency response (see page 6)				
Distortion at $V_{o(rms)}$ = 0.5 V	d_{tot}	<	0.5	%
Volume control range		typ.	75	dB
Signal handling		>	20	mV
Gain variation at V_B decreasing from 7 to 5 V	ΔG_v	typ.	3	dB

Data for use as play-back amplifier (measured at f= 1 kHz)

Voltage gain	G_v		64 ± 2	dB
Frequency response (see page 6)				
Distortion at $V_{o(rms)}$ = 0.5 V	d_{tot}	<	0.5	%
Gain variation at V_B decreasing from 7 to 5 V	ΔG_v	typ.	3	dB



OMVORMER TRANSFORMATOREN

Uitvoering van omvormtransformatoren van verschillende vermogens

De door ons gevoerde omvormertransformatoren zijn opgebouwd uit 'Permax F' en zijn reeds gewikkeld en ingegoten. Deze omvormers blinken uit door o.a.:

- snelle start van de oscillator
- groot uitgangsvermogen
- hoog rendement
- kleine afmetingen
- hoge temperatuurstabiliteit
- eenvoudige (print-) montage
- gunstig prijsniveau

Door bovengenoemde eigenschappen is deze transformator byzonder geschikt voor gebruik bij thyristor-ontstekingen in auto's, als omvormer voor TL-verlichting vanuit de accu, enz.

Door de uitvoering van deze transformator is hij eveneens geschikt voor montage op gedrukte bedradingen.

Deze transformator is uitgevoerd in 6 volt en 12 volt en kan met slechts twee transistoren en enkele weerstanden en condensatoren tot een volwaardige omvormer worden gecompleteerd.

Van Dam Elektronica
Snellemanstraat 10-11 te Rotterdam
Reguliersgracht 105 te Amsterdam

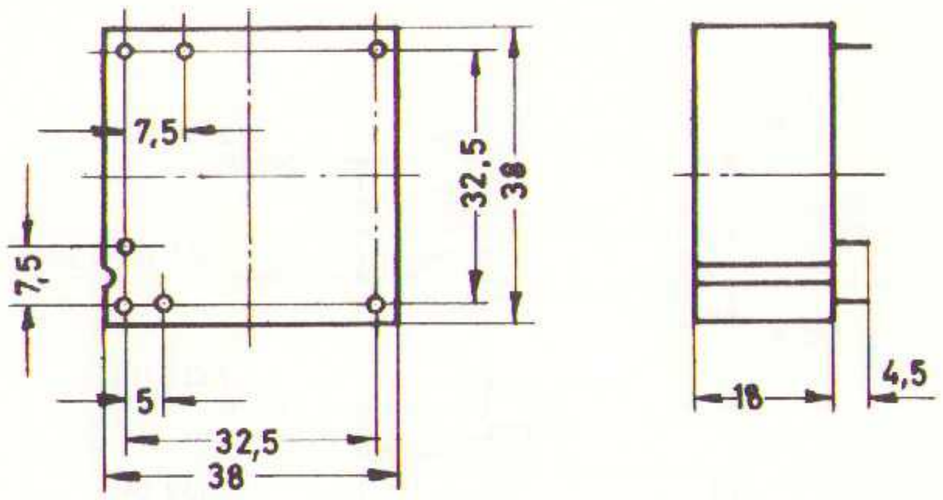
OMVORMER TRANSFORMATOREN

Omvormer transformator voor 6 volt accuspanning: typenummer ZKB416/054-01PF
Omvormer transformator voor 12 volt accuspanning: typenummer ZKB416/058-01PF

Bouwmateriaal:	Uitvoering:	Behuizing:	Afmetingen:	Uitgangsvermogen:
PERMAX F	Printmodel	Ingegoten	38x38x18 mm	circa 30 watt

Maten omvormer transformator
type ZKB416/054-01PF en
type ZKB416/058-01PF

Schaal

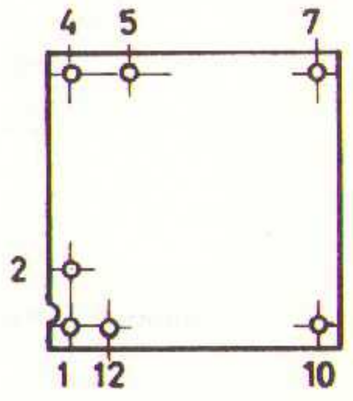


Wikkellingen en aansluitingen:

wikkeling nummer:	draaddoorsnede Ø mm bij 6V	bij 12V
I	0,5	0,5
II	1,2	0,65
III	1,2	0,65
IV	0,5	0,5
V	0,2	0,2

begin/ einde	wikkelingen bij 6V	bij 12V	stift nr
begin	0	0	12
einde	7	7	1
begin	0	0	1
einde	10	20	4
begin	0	0	4
einde	10	20	5
begin	0	0	5
einde	7	7	2
begin	0	0	7
einde	550	550	10

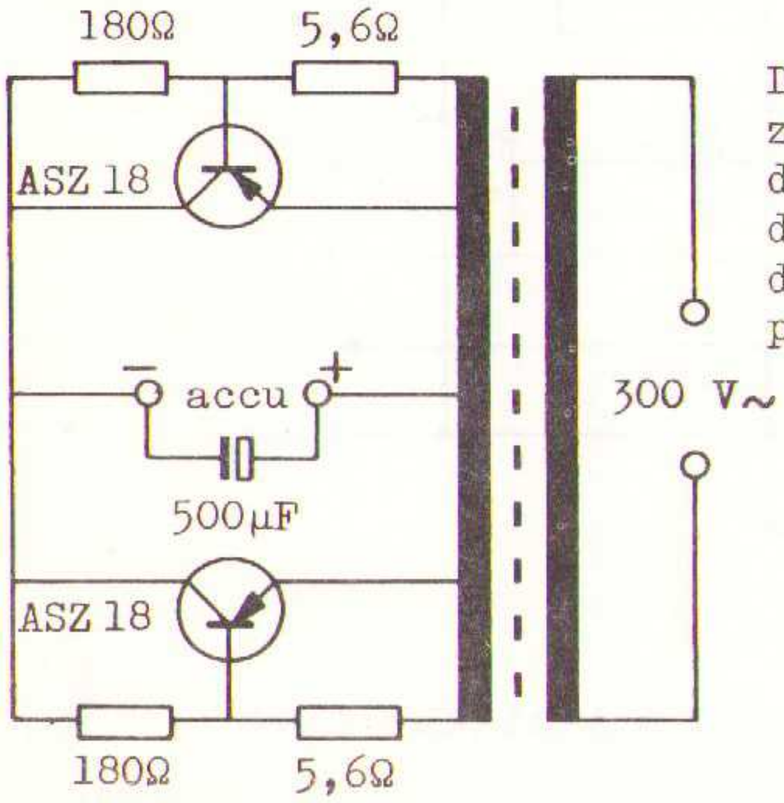
soldeerzijde



Technische gegevens:

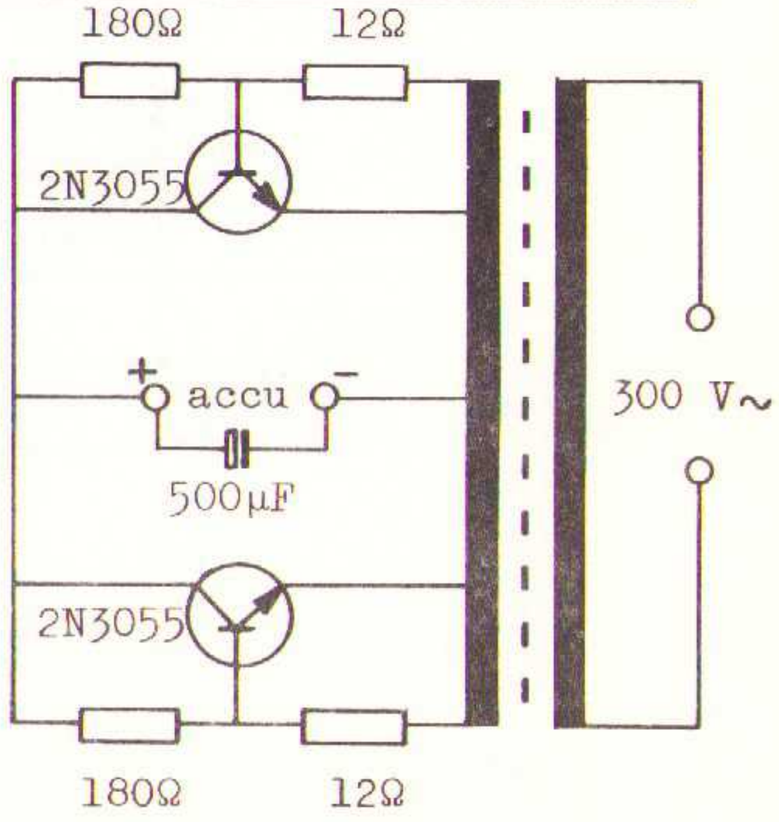
	6 volt	12 volt
accuspanning		
uitgangsspanning	300 volt	300 volt
uitgangsvermogen	ca. 30 watt	ca. 30 watt
werkfrequentie	ca. 2 kHz	ca. 2 kHz
gelijkstroomweerstand van de ingangswikkeling II/III	0,15Ω	0,2Ω
gelijkstroomweerstand van de uitgangswikkeling V	15 Ω	15 Ω
testspanning (f=50Hz) tussen I-IV en V	$2\frac{1}{2}$ kV	$2\frac{1}{2}$ kV

Schakeling voor 6 volt accu:



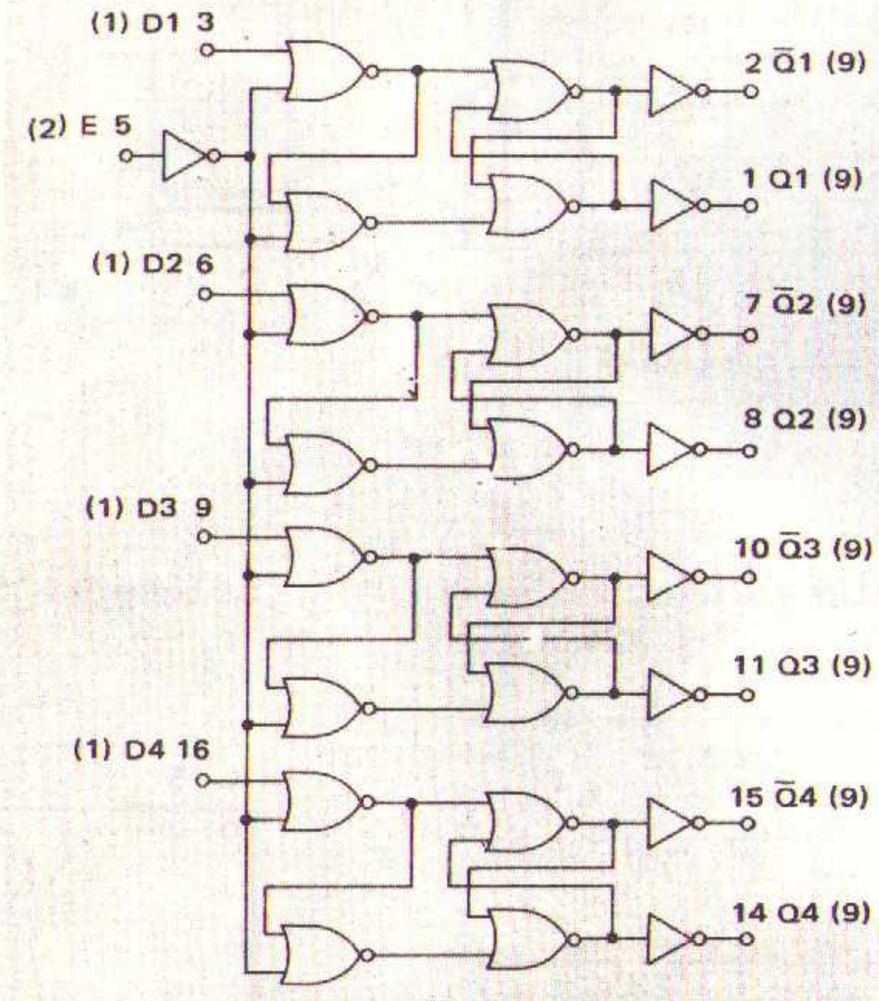
De aangegeven waarden zijn slechts richtwaarden; afhankelijk van de toepassing dienen deze te worden aangepast.

Schakeling voor 12 volt accu:



MC767P • MC867P

JANUARY 1969



Number in Parenthesis Indicates Loading Factor.

The MC767P/867P Quad Latch is designed for use in any application requiring temporary storage. A common enable line allows only the desired information to be "clocked in." When the level of the enable line is high, the output of each latch will be synonymous with the data input to that latch. When the enable line level goes low, the output will remain at the previous level, independent of any changes at the input. The MC767P/867P is available in a 16-pin dual in-line plastic package.

TRUTH TABLE

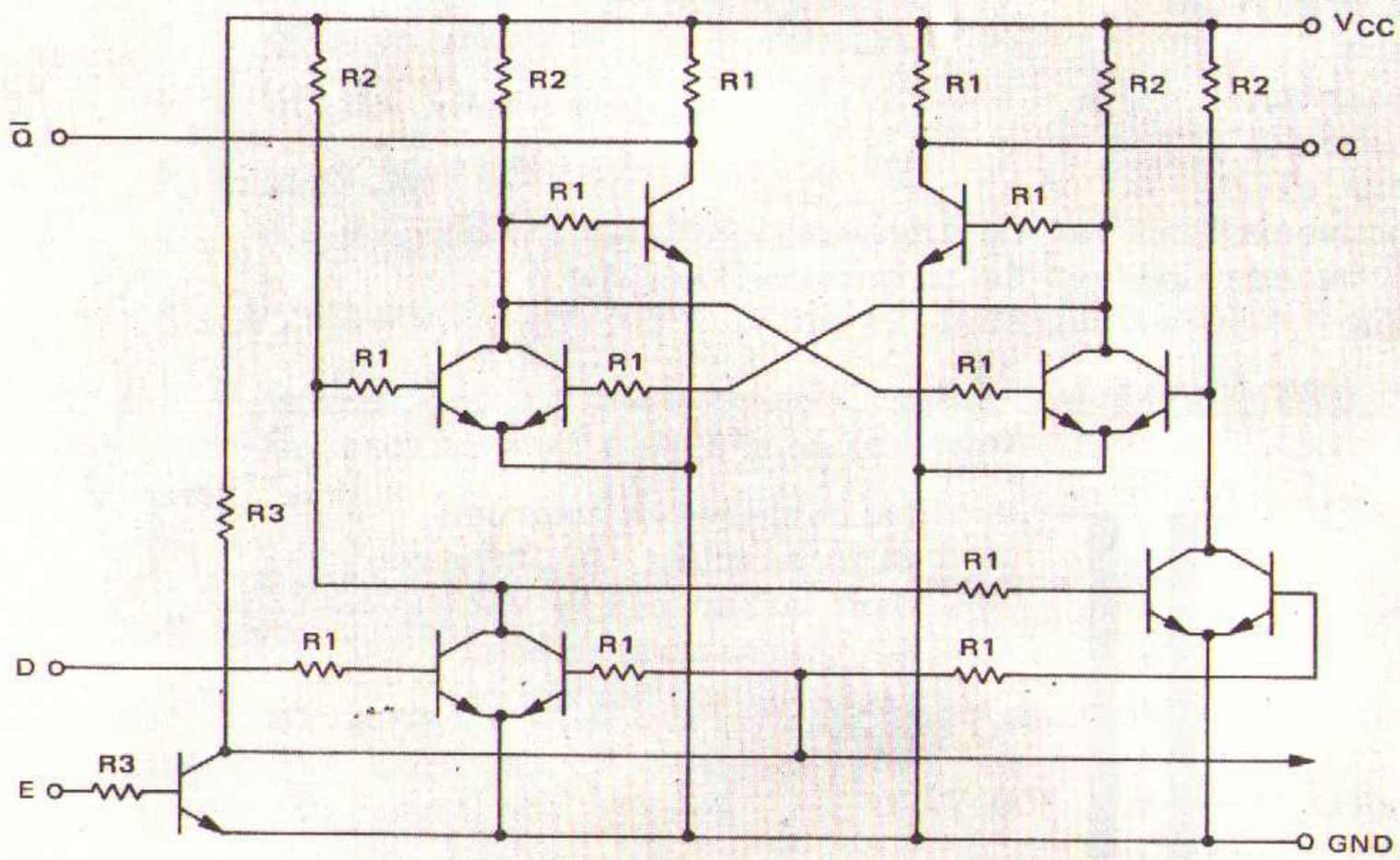
E	D	Q_{n+1}	$\bar{Q}_{n+1}$
0	0	Q_n	$\bar{Q}_n$
0	1	Q_n	$\bar{Q}_n$
1	0	0	1
1	1	1	0

$t_{pd(avg)}$* = 50 ns typ

P_D = 110 mW typ

$$*\text{Avg } t_{pd} = \frac{t_{on} + t_{off}}{2}$$

1/4 OF CIRCUIT SHOWN



TYPICAL RESISTANCE VALUES

R1 = 1.5 k R3 = 750 Ω

R2 = 3.6 k

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one latch. The other latches are tested in the same manner.

@ Test Temperature		TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
MC867P	0°C	0.880	0.850	1.80	0.500	3.60
	+25°C	0.830	0.800	1.80	0.460	3.60
	+75°C	0.740	0.710	1.80	0.400	3.60
MC767P	+15°C	0.865	0.865	1.80	0.475	3.60
	+25°C	0.850	0.850	1.80	0.460	3.60
	−55°C	0.800	0.800	1.80	0.430	3.60

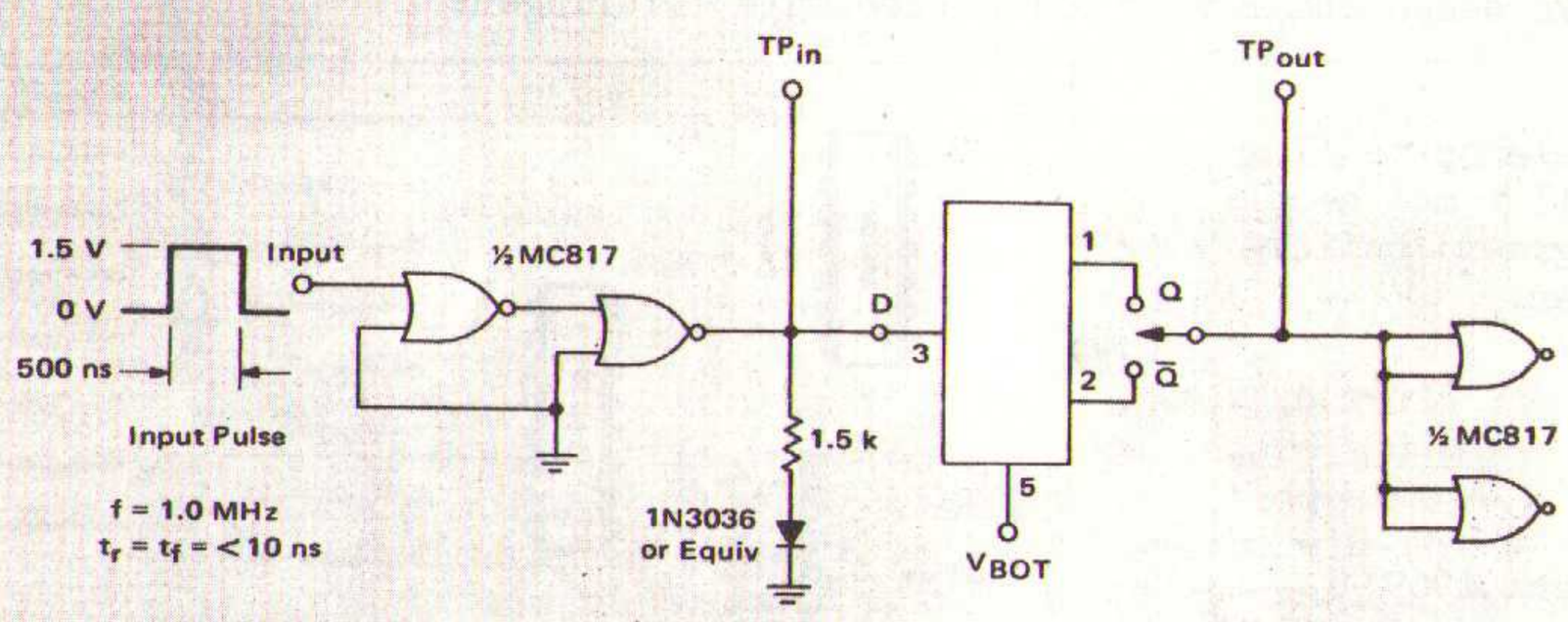
Characteristic	Symbol	Pin Under Test	MC867P Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	MC767P Test Limits +15°C Min	+15°C Max	+25°C Min	+25°C Max	+55°C Min	+55°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Gnd
Input Current	I_{in}	3	-	150	-	140	-	140	μAdc	-	150	-	150	-	150	μAdc	3	-		-	13	4,5
	$2\,I_{in}$	5	-	300	-	280	-	280	μAdc	-	300	-	300	-	300	μAdc	5	-		-	13	4
Output Current	I_{A9}	1	-1.28	-	-1.28	-	-1.20	-	mAdc	-1.28	-	-1.28	-	-1.28	-	mAdc	3,5	1	-	-	13	4
		2	-1.28	-	-1.28	-	-1.20	-	mAdc	-1.28	-	-1.28	-	-1.28	-	mAdc	5	2	-	-	13	3,4
Saturation Voltage	$V_{CE(sat)}$	1	-	250	-	250	-	250	mVdc	-	220	-	230	-	320	mVdc	5	-	-	-	13	3,4
		2	-	↓	-	↓	-	↓		-	↓	-	↓	-	↓	↓	3,5	-	-	-	↓	4
		1	-		-		-			-		-		-			3,5*	-	-	-		3,4,5*
		2	-		-		-			-		-		-			3,5**	-	-	-		3,4,5**
Power Supply Drain Current	I_{PD}	13	-	-	-	35	-	-	mAdc	-	-	-	35	-	-	mAdc	-	-	-	-	13	4,5
																	Pulse In	Pulse Out				
Switching Times	t_{3+1+}	1	-	-	-	75	-	-	ns	-	-	-	75	-	-	ns	3	1	5	-	13	4
	t_{3-1-}	1	-	-	-	70	-	-	↓	-	-	-	70	-	-	↓	↓	1	↓	-	↓	↓
	t_{3+2-}	2	-	-	-	90	-	-		-	-	-	90	-	-			2		-		
	t_{3-2+}	2	-	-	-	60	-	-		-	-	-	60	-	-			2		-		

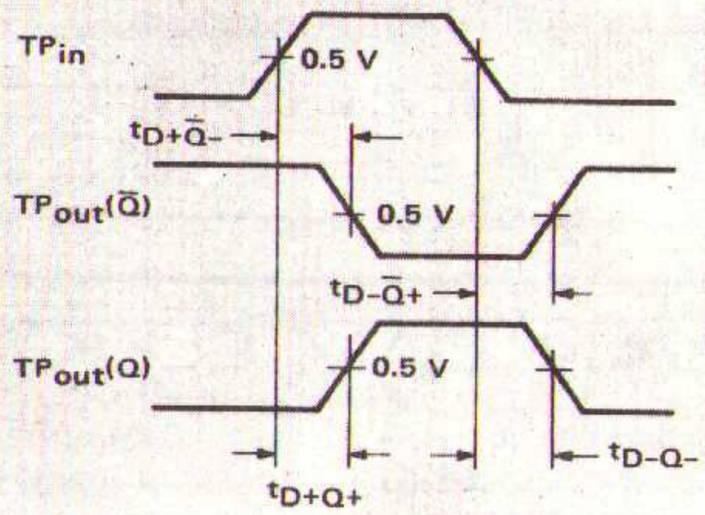
Ground inputs of latches not under test. Other pins not listed are left open.

*A negative pulse from V_{in} to ground is applied to pin 5, then 2.0 ms later a positive pulse from ground to V_{in} is applied to pin 3 for measurement of V_{CE} on pin 1.

**A negative pulse from V_{in} to ground is applied to pin 5, then 2.0 ms later a positive pulse from V_{in} to ground is applied to pin 3 for measurement of V_{CE} on pin 2.

SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS





Uw leverancier: Van Dam Elektronica - Rotterdam - Amsterdam

TIENTELLER MET GEÏNTEGREERD BUFFER•GEHEUGEN

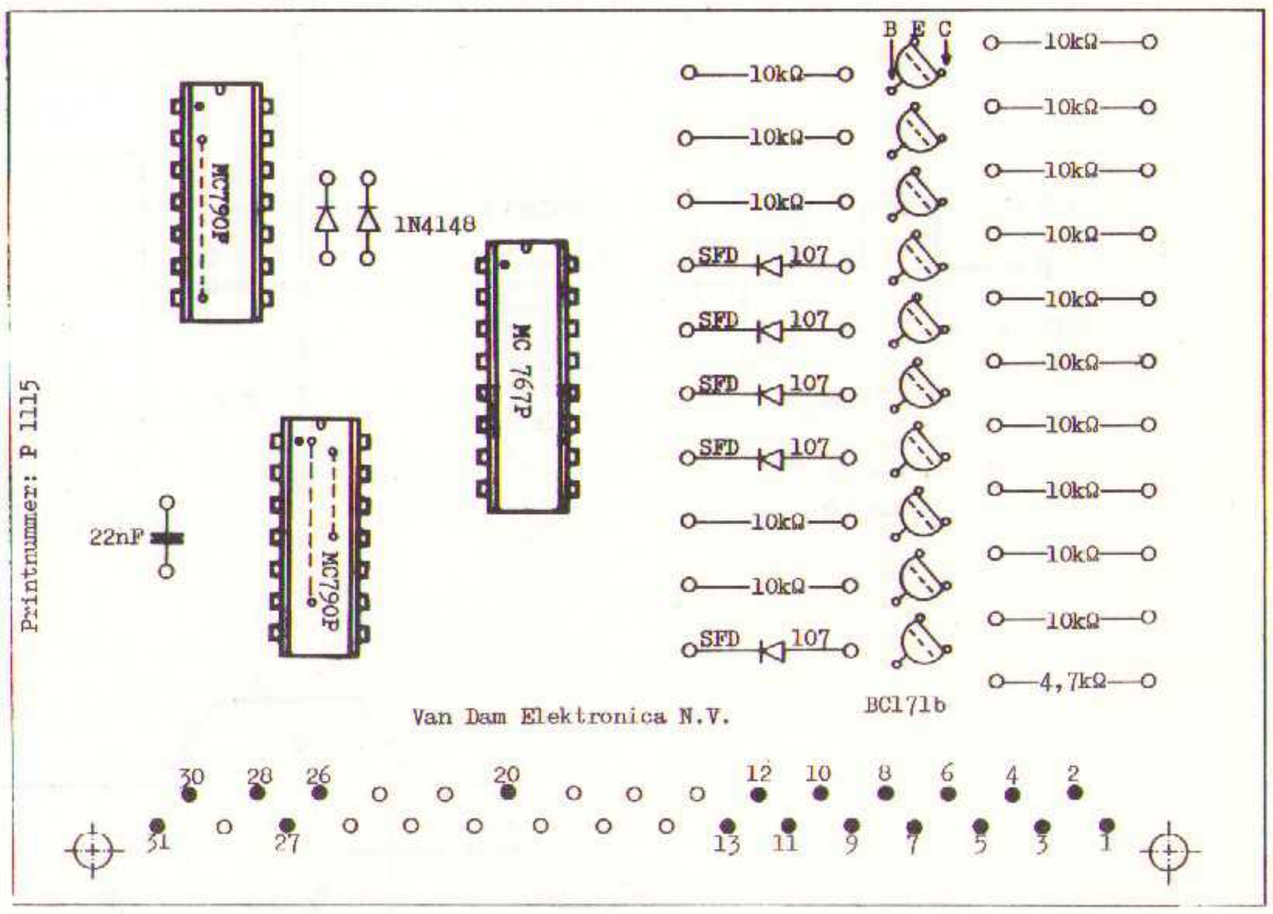
Na een teller met een elektronisch geheugen, opgebouwd uit discrete componenten, hebben wij nu ook een teller met een geïntegreerd buffergeheugen ontwikkeld. Hierin wordt gebruik gemaakt van de nieuwe geïntegreerde schakeling MC 767P van Motorola, waardoor voor het geheugen nog slechts 15 i.p.v. 80 soldeerpunten aanwezig zijn. Bovendien zijn betere specificaties mogelijk, doordat vanuit het geheugen geen stroom meer wordt toegevoerd aan de tienteller; dit geeft betere specificaties voor de maximaal toelaatbare telfrequentie. De aansluitingen van deze nieuwe teller komen volledig overeen met de in onze technische documentatie deel 1, blz. 9-10 beschreven uitvoering.

Voor deze nieuwe teller gelden de volgende specificaties:

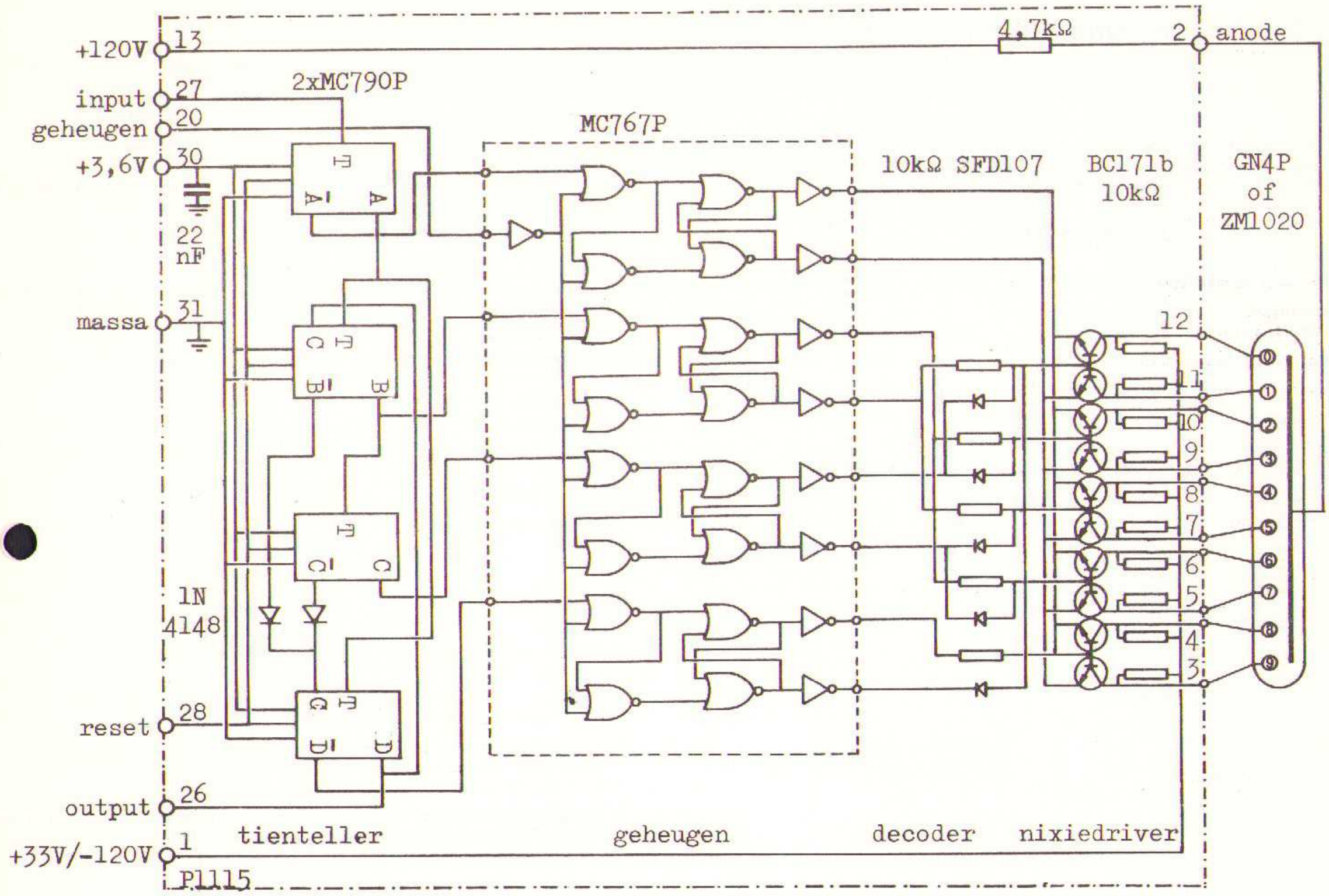
- telfrequentie van DC tot 10 MHz.
- noodzakelijke spanningsvorm telingang: blokvormig.
- stroomverbruik: +3,6 volt: circa 90 mA.
  +33 volt: circa 3 mA.
  +120 volt: circa 1,8 mA.
- toelaatbare ingangsspanningen: ingang (punt 27) +3,6 volt (factor 5).
  reset (punt 28) +3,6 volt (factor 6).
  geheugen (punt 20) +3,6 volt (factor 2).
- beschikbare uitgangsspanningen: teller (punt 26) ca. 1 V. (factor 7).
  nixiedriver (pt.3-12) ca.33 V. (max. $\frac{1}{2}$mA).
- printafmetingen: 100 x 70 mm, materiaal: glasvezel.
- geschikt voor gebruik 31 polige connector en printgeleiders.

Opmerking: bij de opgegeven beschikbare stroom van de nixiedriver is het stroomverbruik van de nixiebuis buiten beschouwing gebleven. Deze stroom van $\frac{1}{2}$mA is derhalve beschikbaar voor extra (decimale) sturingen.

Onderdelenopstelling tienteller met een geïntegreerd buffergeheugen.



TIENTELLER MET GEïNTEGREERD BUFFER•GEHEUGEN



Van Dam Elektronica - Holland

Aansluitingen.

punt 31 gaat naar massa.
punt 30 gaat naar +3,6 volt.
punt 28 gaat naar de reset van de tijdeenheid en van de andere tellers.
punt 27 gaat naar uitgang vorige teller of uitgang van de tijdeenheid.
punt 26 gaat naar de ingang van de volgende teller of overbereik-indicator.
punt 20 gaat naar doorgeefpunt tijdeenheid of via druktoets naar +3,6 volt.
punt 13 gaat naar +120 volt.
punt 12 gaat naar 0 van de cijferbuis.
punt 11 gaat naar 1 van de cijferbuis.
punt 10 gaat naar 2 van de cijferbuis.
punt 9 gaat naar 3 van de cijferbuis.
punt 8 gaat naar 4 van de cijferbuis.
punt 7 gaat naar 5 van de cijferbuis.
punt 6 gaat naar 6 van de cijferbuis.
punt 5 gaat naar 7 van de cijferbuis.
punt 4 gaat naar 8 van de cijferbuis.
punt 3 gaat naar 9 van de cijferbuis.
punt 2 gaat naar anode van cijferbuis.
punt 1 gaat naar +33 volt en -120 volt van de voeding of andere tellers.

BRY39

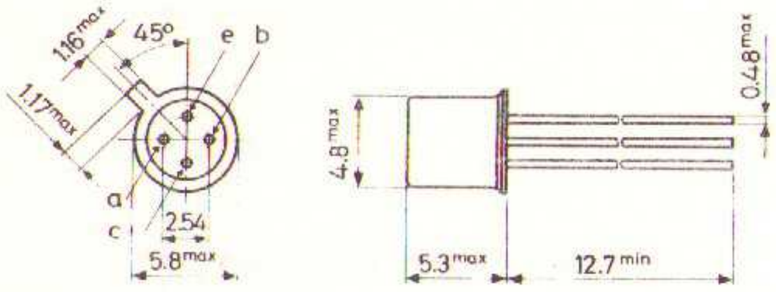
SILICON CONTROLLED SWITCH

The BRY39 is a planar p-n-p-n switch in a TO-72 metal envelope, intended as driver for numerical indicator tubes and other switching applications.
It is an integrated pnp-npn transistor pair of which all electrodes are accessible. The collector of the n-p-n transistor is connected to the case.

QUICK REFERENCE DATA				
P-N-P transistor				
Emitter-base voltage (open collector)	$-V_{EBO}$	max.	70	V
N-P-N transistor				
Collector-base voltage (open emitter)	V_{CBO}	max.	70	V
Emitter current (peak value)	$-I_{EM}$	max.	500	mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	250	mW
Junction temperature	T_j	max.	150	°C
Forward on-state voltage				
I_A = 50 mA; I_C = 0; R_{BE} = 10 kΩ	V_{AE}	<	1.4	V
Holding current				
I_C = 10 mA; $-V_{BB}$ = 2 V; R_{BE} = 10 kΩ	I_H	<	1.0	mA
Turn on time	t_{on}	<	0.25	μs
Turn off time	t_q	<	5.0	μs

MECHANICAL DATA Dimensions in mm

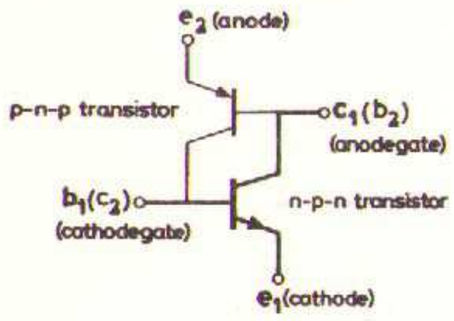
Collector connected to case
TO-72



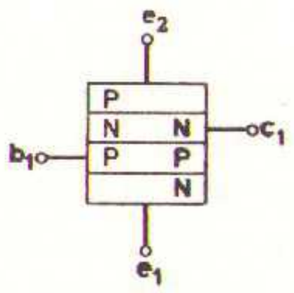
Accessories available: 56246; 56263.

MEANING OF SYMBOLS, used in the schematic presentation of the S.C.S.

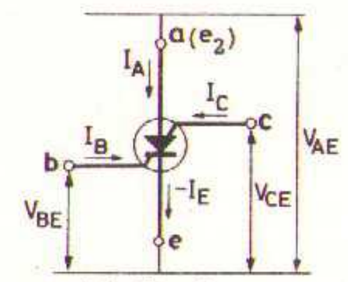
2 transistors equivalent circuit
n-p-n transistor + p-n-p transistor



p-n-p-n S.C.S. equivalent circuit



S.C.S. symbol



a = anode (emitter of p-n-p transistor)

CHARACTERISTICS T_j = 25 °C unless otherwise specified

INDIVIDUAL N-P-N TRANSISTOR

Collector cut-off current

V_{CE} = 70 V; R_{BE} = 10 kΩ	I_{CER}	<	100 nA
V_{CE} = 70 V; R_{BE} 10 kΩ; T_j = 150 °C	I_{CER}	<	10 μA

Emitter cut-off current

I_C = 0; V_{EB} = 5 V; T_j = 150 °C	I_{EBO}	<	10 μA

RATINGS (Limiting values) [1])

Voltages			p-n-p	n-p-n	
Collector-base voltage (open emitter)	V_{CBO}	max.	−70	70 [2])	V
Collector-emitter voltage (R_{BE} = 10 kΩ)	V_{CER}	max.		70 [2])	V
Collector-emitter voltage (open base)	V_{CEO}	max.	−70		V
Emitter-base voltage (open collector)	V_{EBO}	max.	−70 [2])	5 [3])	V
Currents					
Emitter current (d.c.)	I_E	max.	100	−100	mA
Emitter current (peak value) $t_p \leq 1$ ms; $\delta \leq 0.05$	I_{EM}	max.	500	−500	mA
Collector current (d.c.)	I_C	max.		50	mA
Collector current (peak value)	I_{CM}	max.		100 [4])	mA
Power dissipation					
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.		250	mW
Temperatures					
Storage temperature	T_{stg}		−65 to + 200		°C
Junction temperature	T_j	max.		150	°C

THERMAL RESISTANCE

From junction to ambient	$R_{th\ j\text{-}a}$	=	0.5 °C/mW

1) Limiting values according to the Absolute Maximum System as defined in IEC publication 134.

2) In numerical indicator tube driver circuits higher voltages are allowed, provided the collector current does not exceed a d.c. current of 1 mA.

3) In numerical indicator tube driver circuits higher voltages are allowed during the discharge of a capacitor of max. 390 pF, provided the charge does not exceed 50 nC and the current is limited to 150 mA.

4) During switching-on, the device can withstand a discharge of a capacitor of max. 500 pF. This capacitor is charged, when the transistor is in cut-off condition, with a collector supply voltage of 160 V with a series resistance of 100 kΩ.

CHARACTERISTICS (continued) T_j = 25 °C unless otherwise specified

INDIVIDUAL N-P-N TRANSISTOR

Saturation voltages

I_C = 10 mA; I_B = 1 mA	V_{CEsat}	<	500 mV
	V_{BEsat}	<	900 mV

D.C. current gain

I_C = 10 mA; V_{CE} = 2 V	h_{FE}	>	50

Transition frequency

I_C = 10 mA; V_{CE} = 2 V	f_T	typ.	300 MHz

Collector capacitance

$I_E = I_e$ = 0; V_{CB} = 20 V	C_c	<	5 pF

Emitter capacitance

$I_C = I_c$ = 0; V_{EB} = 1 V	C_e	<	25 pF

INDIVIDUAL P-N-P TRANSISTOR

Collector cut-off current

I_B = 0; $-V_{CE}$ = 70 V; T_j = 150 °C	$-I_{CEO}$	<	10 μA

Emitter cut-off current

I_C = 0; $-V_{EB}$ = 70 V; T_j = 150 °C	$-I_{EBO}$	<	10 μA

D.C. current gain

I_E = 1 mA; V_{CB} = 0	h_{FE}		0.25 to 2.5

COMBINED DEVICE

Forward voltage at R_{BE} = 10 kΩ

I_A = 50 mA; I_C = 0	V_{AE}	<	1.4 V
I_A = 50 mA; I_C = 0; T_j = −55 °C	V_{AE}	<	1.9 V
I_A = 1 mA; I_C = 10 mA	V_{AE}	<	1.2 V

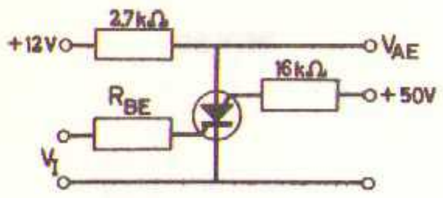
Holding current at R_{BE} = 10 kΩ

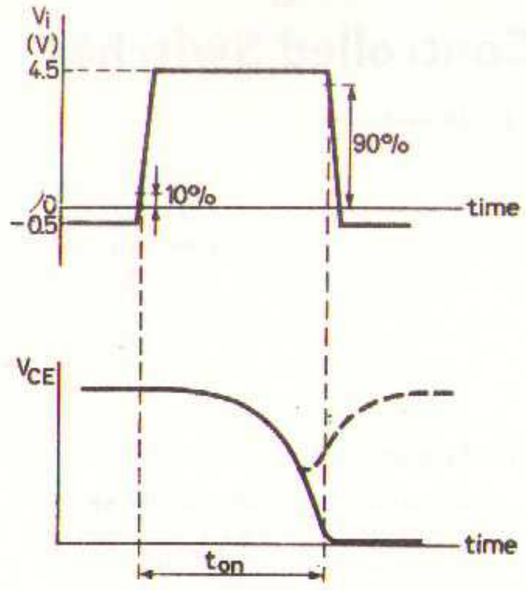
I_C = 10 mA; $-V_{BB}$ = 2 V	I_H		0.1 to 1.0 mA

CHARACTERISTICS (continued) Tj = 25 °C unless otherwise specified

SWITCHING TIMES see also page 6

Turn on time when switched from
$-V_{BE}$ = 0.5 V to $+V_{BE}$ = 4.5 V; R_{BE} = 1 kΩ t_{on} < 0.25 μs
R_{BE} = 10 kΩ t_{on} ≤ 1.5 μs

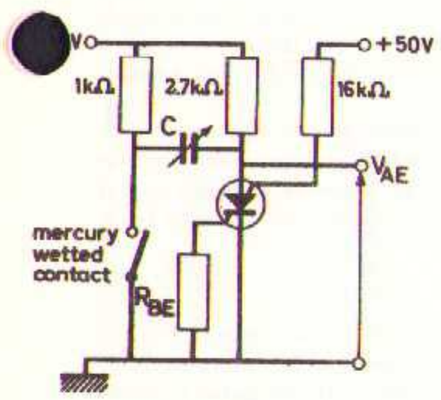


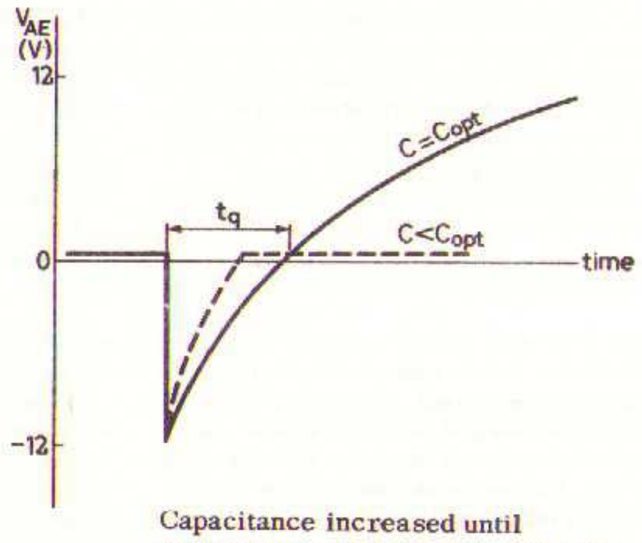


Pulse duration increased until dashed curve disappears

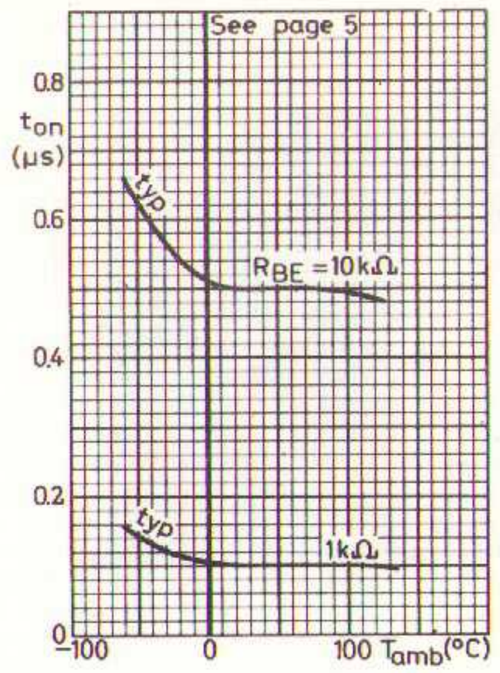
Turn off time

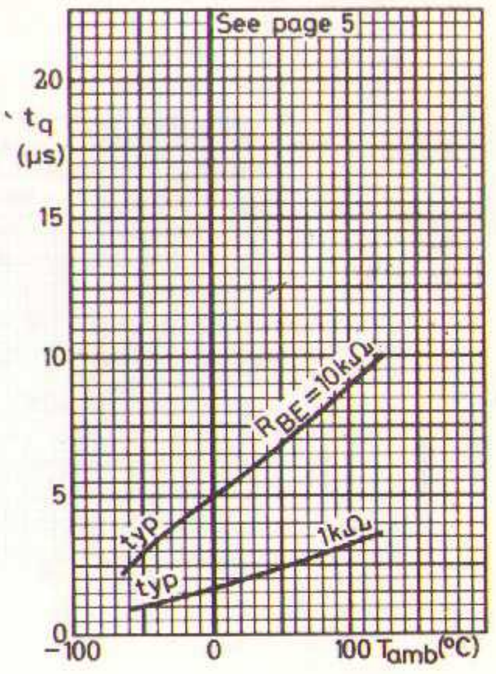
R_{BE} = 1 kΩ t_q < 5 μs
R_{BE} = 10 kΩ t_q < 8 μs
T_j = 125 °C; R_{BE} = 10 kΩ t_q < 15 μs

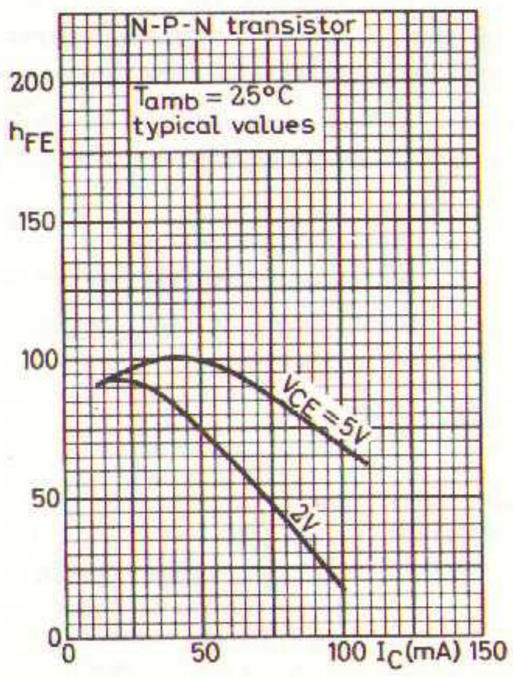


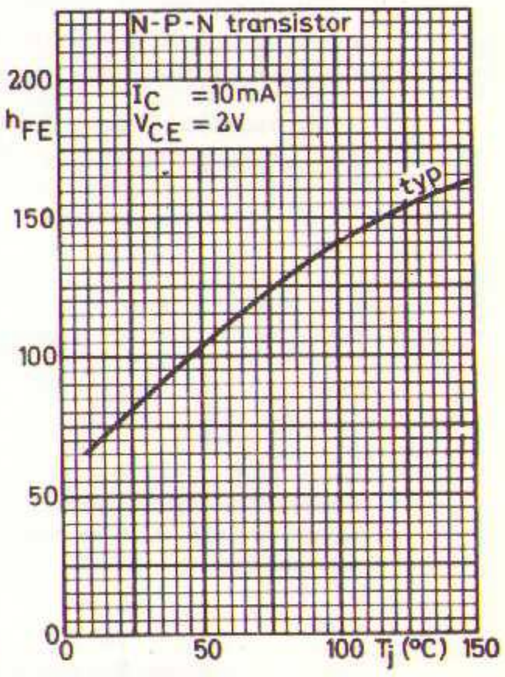


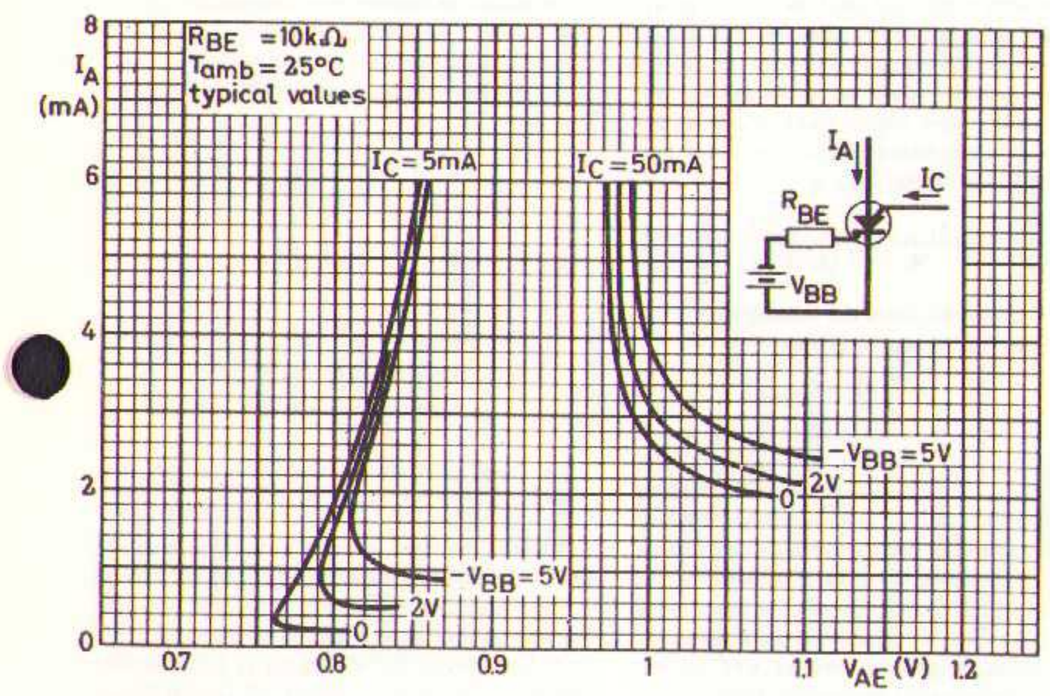
Capacitance increased until dashed curve disappears at C = C_{opt}

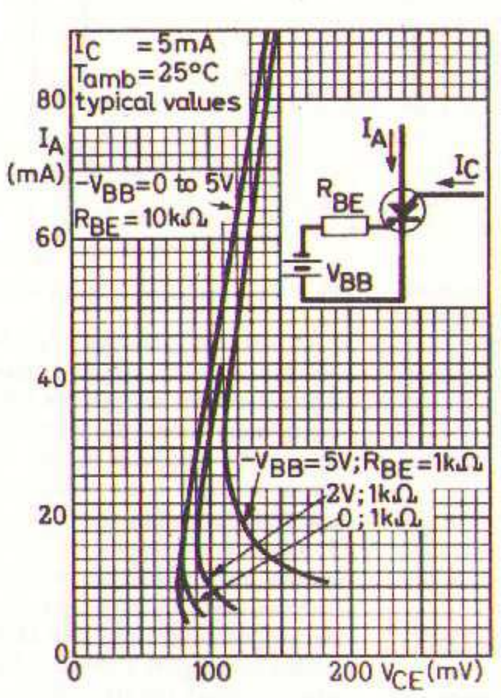


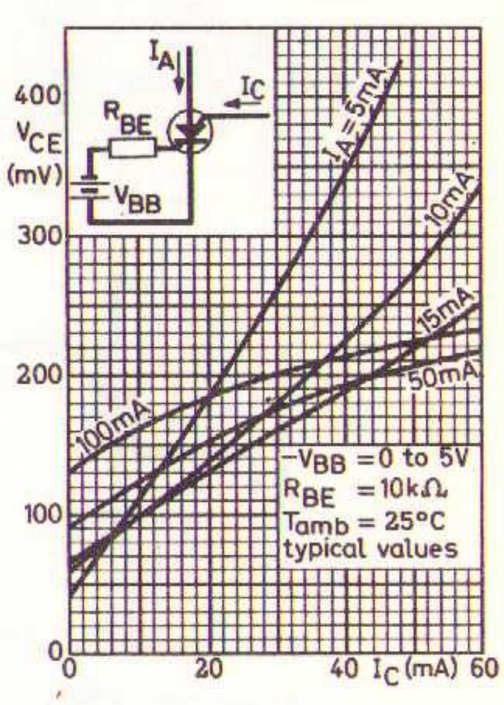


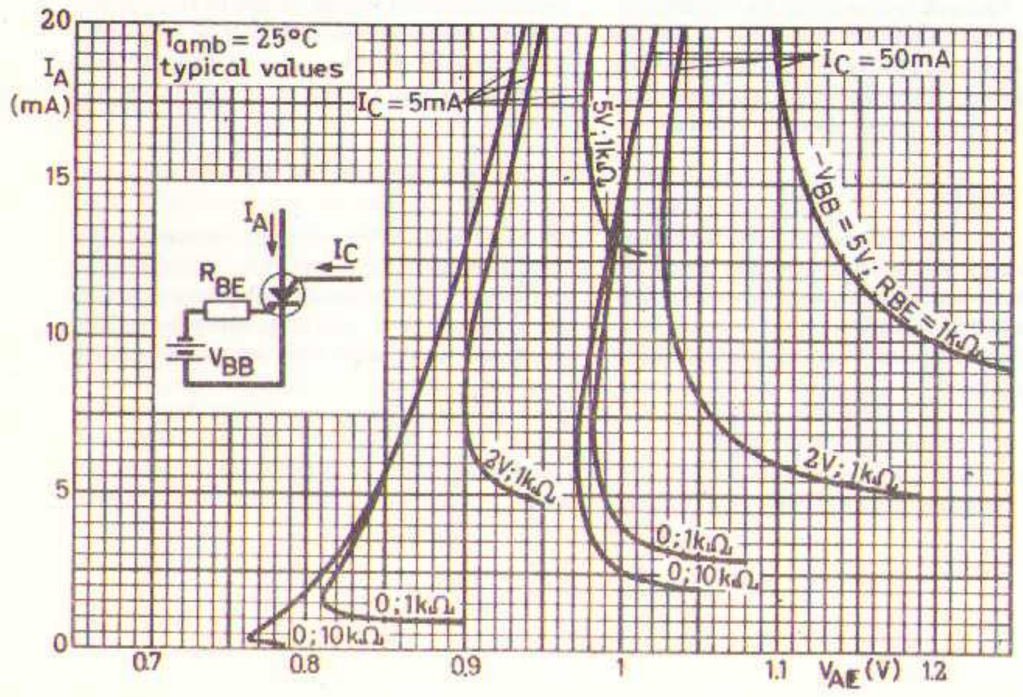


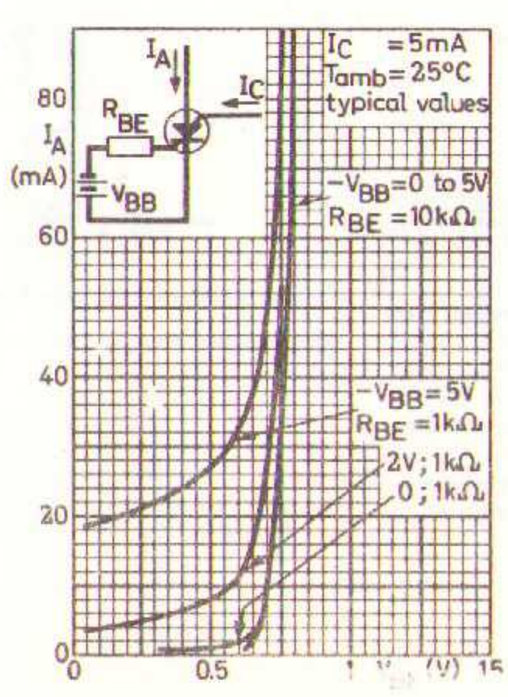


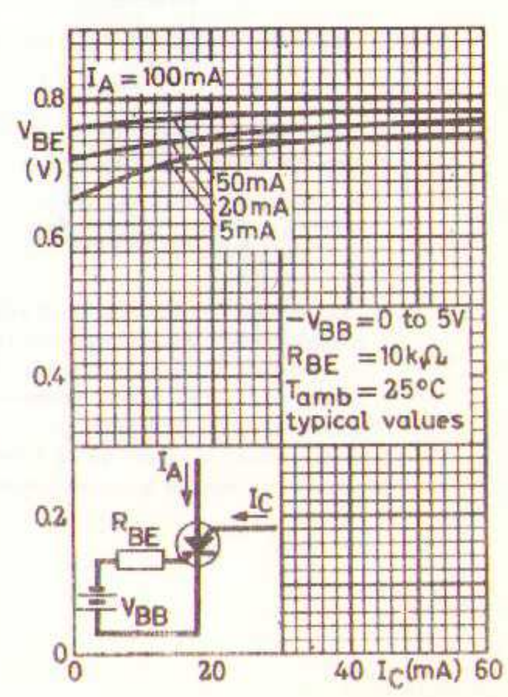


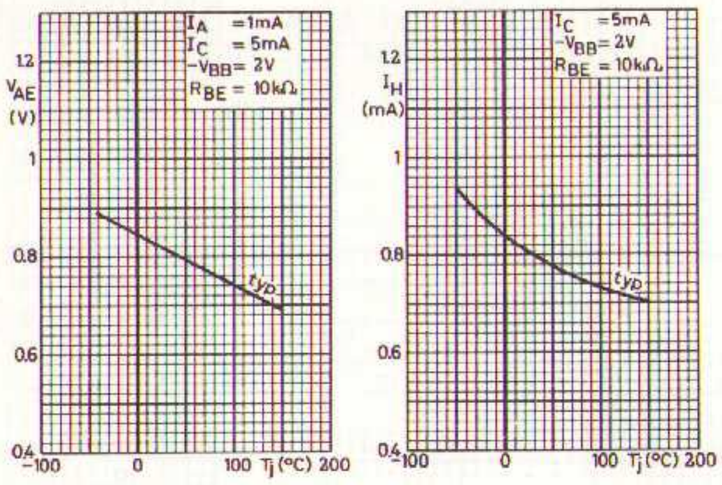












Op de navolgende pagina's zijn verschillende schakelingen opgenomen met de BRY 39, waarvoor qua mogelijkheden én qua prijs een groot aantal interessante toepassingsgebieden aanwezig is. Ook bij modelbesturing leent deze thyristor-tetrode zich voor interessante experimenten. Deze documentatie bestaat uit een volledige overdruk uit "Application Information" nummer 325 en vol. 21 nr. 1, 1966-1967 en is ons beschikbaar gesteld door N.V. Philips' Gloeilampenfabrieken te Eindhoven.

Circuit Logic with Silicon Controlled Switches

BRY 39

D. J. G. Janssen*

Equations governing the movement of charge carriers in the n-p-n-p structure of a silicon controlled switch are given and its electrical behaviour is described, comparisons being drawn with the operation of more familiar semiconductor devices such as thyristors and transistors.
To illustrate the wide range of applications of the silicon controlled switch, a number of circuits are taken up; these include ring counters, driving circuits for numerical indicator tubes and print-out devices and several gate circuits.

Introduction

A silicon controlled switch, of which the BRY39 is a typical example, is a p-n-p-n semiconductor device that structurally resembles a small thyristor, except that all four electrodes are accessible. Functionally it is comparable to a low-power transistor combined with a holding circuit. As will be shown, the interaction and accessibility of the four electrodes opens new and advantageous ways to the performance of many switching and logic operations for which two or more active elements would otherwise be needed. Fairly large currents can be switched, and the simplicity of the circuits makes for economy as well as reliability. Before going into circuit details, the operating theory will be discussed with reference to structure and the movement of charge carriers across the several junctions.

Structure and Operating Theory

Fig. 1*a* shows, schematically, the internal structure and Fig. 1*b* the conventional symbol and electrode designations of a silicon controlled switch (abbreviated "SCS"): emitter E (sometimes called cathode), base B (sometimes cathode gate), collector C (sometimes anode gate) and anode A.

For explanatory purposes, the structure shown may be taken to consist of a first (n-p-n) transistor with emitter E, base B and collector C and a second (p-n-p) transistor the emitter, base and collector of which are formed by electrodes A, C and B respectively.

Two steady states are possible, and in both equilibrium is maintained by a leakage current across the common junction J_2. Moreover, a fraction $\alpha_1 I_E$ of the emitter current and a fraction $\alpha_2 I_A$ of the anode current flow through this junction, α_1 and α_2 being respectively functions of the currents through the n-p-n and the p-n-p transistor.

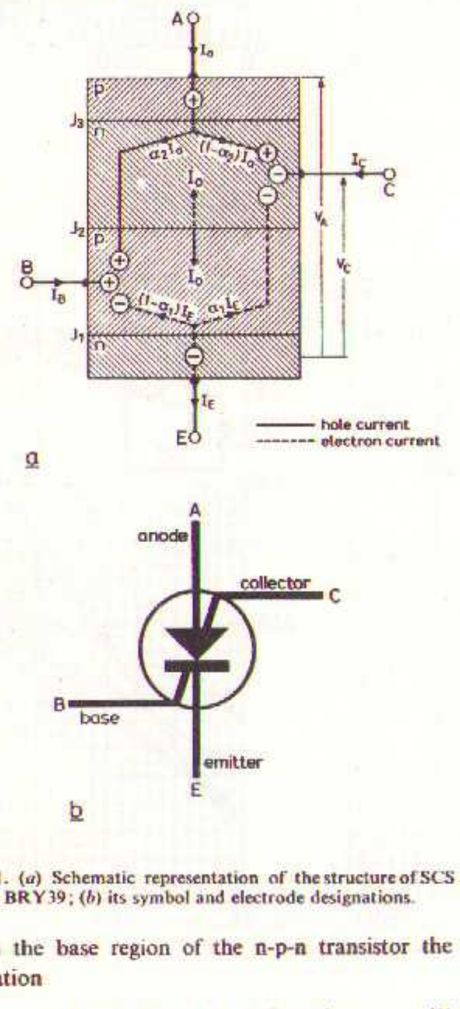


Fig. 1. (*a*) Schematic representation of the structure of SCS Type BRY39; (*b*) its symbol and electrode designations.

In the base region of the n-p-n transistor the equation

$$(1-\alpha_1)I_E = \alpha_2 I_A + I_B + I_o, \qquad (1)$$

and in the collector region the equation

$$(1-\alpha_2)I_A = \alpha_1 I_E - I_C + I_o, \qquad (2)$$

describing the recombination of charge carriers, must be fulfilled. From eqs (1) and (2):

$$I_C = \frac{1}{1-\alpha_1}\cdot I_o + \frac{\alpha_1}{1-\alpha_1}\cdot I_B + \frac{\alpha_1+\alpha_2-1}{1-\alpha_1}\cdot I_A. \qquad (3)$$

As a rule the first term is so small with respect to the others that eq. (3) may be simplified to:

$$I_C \simeq \frac{\alpha_1}{1-\alpha_1}\cdot I_B + \frac{\alpha_1+\alpha_2-1}{1-\alpha_1}\cdot I_A. \qquad (4)$$

As long as voltage V_C exceeds V_A, junction J_3 is reverse-biased so that the p-n-p transistor is cut off and I_A becomes negligibly small. The second term of eq. (4) can then be disregarded and the SCS operates as a normal n-p-n silicon planar transistor with emitter E, base B and collector C (see Fig. 2).

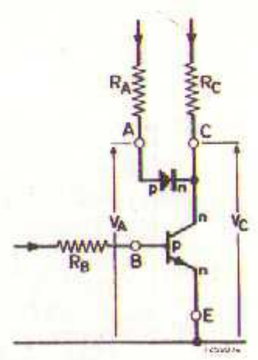


Fig. 2. Equivalent circuit of an SCS in the case of $V_C > V_A$.

If, now, a current pulse $+I_B$ is fed into the base, which is normally negatively biased, the resulting collector current will raise the voltage drop across the collector resistor R_C, so that V_C decreases. As soon as V_C falls below V_A, the simple equivalent circuit of Fig. 2 is no longer applicable, because the diode formed by the anode-collector junction J_3 is then forward biased; the sum of α_1 and α_2 now exceeds unity so that the second term of eq. (4) becomes positive. The p-n-p transistor formed by the anode, collector and base of the SCS is then rendered conductive as shown in Fig. 3. The current passing through this transistor flows back into the base of the n-p-n transistor, so that the original base current $+I_B$ is augmented. This raises the collector current I_C which — by virtue of the increased base current of the p-n-p transistor — leads to a further increase of the current flowing through the SCS. This process continues until the collector-to-emitter voltage and the anode-to-emitter voltage have reached their saturation values and the SCS is in the ON state.

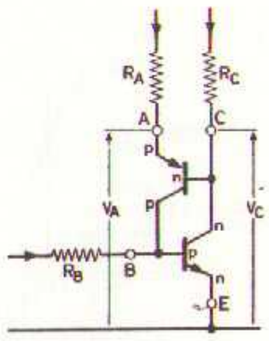


Fig. 3. Equivalent circuit of an SCS in the case of $V_A > V_C$.

Since the current that keeps the n-p-n transistor in the ON state is supplied by the p-n-p transistor, the SCS remains in this state after the positive-going base current pulse has ceased. Eq. (4) reveals that the value of I_A which is required to keep the SCS in the ON state (termed the holding current I_H) depends on the external reverse base current $-I_B$. It can be derived from this equation that the condition for keeping the SCS in the ON state is:

$$I_H > \left(I_C - \frac{\alpha_1}{1-\alpha_1}\cdot I_B\right)\left(\frac{1-\alpha_1}{\alpha_1+\alpha_2-1}\right). \qquad (5)$$

For most practical purposes the holding current of the SCS Type BRY39 may be taken to be:

$$I_H > (I_C - 50I_B)/20. \qquad (6)$$

Because the ON state is maintained by the anode once a short driving pulse has been applied to the base (usually via a capacitance), an SCS might be considered as a transistor incorporating a holding circuit, no continuous driving current being required to keep it in the ON state. This use of the anode as a control electrode explains why the output signal of an SCS is commonly taken from the collector.

The common procedure to return the SCS to the OFF-state is to reduce I_A temporarily below I_H. To this end a negative voltage is usually applied to the anode so that the direction of I_A is momentarily reversed. The anode-collector junction J_3 then becomes reverse-biased after about 0.1 μs and the situation represented in Fig. 2 is restored. The base being negatively biased, an n-p-n transistor with reverse base current is thus obtained, which is completely cut off within a few microseconds. The sum of these two intervals is termed the "turn-off time".

By analogy with the procedure applied to thyristors designed for gate turn-off, it might be supposed that an alternative way to return the SCS to the OFF state would be to raise the negative base current $-I_B$ until the current left for driving the n-p-n transistor became insufficient. This method is impracticable, however, because the voltage drop produced by $-I_B$ across the internal base resistance would usually exceed the permissible maximum of −5 V across the base-emitter junction J_1.

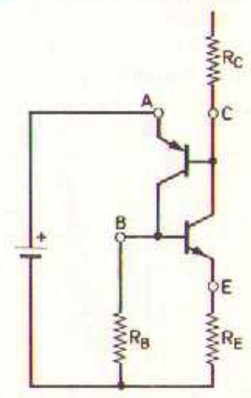


Fig. 4. Circuit configuration which allows the SCS to be switched off by raising the collector current.

There is, however, another method of switching off an SCS, namely by raising the collector current I_C. For practical reasons this is feasible only if a suitable resistor R_E is included in the emitter circuit, as shown in Fig. 4. As long as anode current still flows, the emitter current will remain almost constant, equalling the difference between the supply voltage and the substantially constant anode-to-emitter saturation voltage, divided by the resistance R_E. The collector current can thus be increased at the expense of the anode current until the latter drops below the holding value and the SCS is switched off.

Basic Circuits

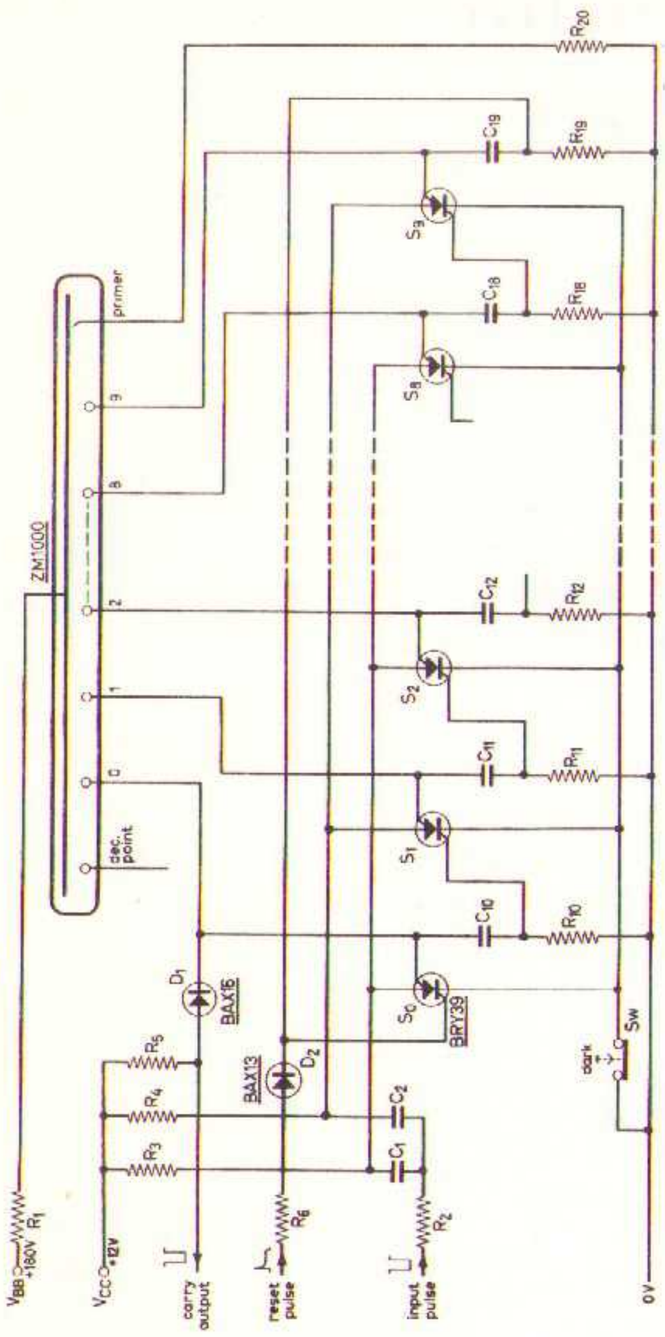
Although the variety of circuits in which the BRY39 can advantageously be used precludes giving an exhaustive survey, those discussed below may suffice to indicate its versatility.

It should be recognised that, except in the circuits of Figs 5 and 13, the component values are to be considered as merely directive, no attempt having been made to render the designs optimal. In fact, the optimum design is usually governed by external conditions which differ from case to case, such as

* Philips Elcoma Division, Central Application Laboratory, Eindhoven.

required speed and expected deviations of the supply voltages and input signals from their nominal values. The circuits shown can easily be adapted to these variations.

Ring Counter with Numerical Indicator Tube ZM1000



R_1	15 kΩ ±3%
R_2	1 kΩ ±5%
R_3	5.1 kΩ ±5%
R_4	5.1 kΩ ±5%
R_5	10 kΩ ±5%
R_6	2.2 kΩ ±5%
R_{10}-R_{19}	1 kΩ ±5%
R_{20}	10 MΩ ±5%
C_1, C_2	4.7 nF ±10%
C_{10}-C_{19}	390 pF ±10%

Fig. 5. Ring counter with numerical indicator tube ZM1000 (optimum design for V_{BB} = 180 V ±5% and V_{CC} = 12 V ±15%).

The SCS Type BRY39 makes it possible to build ring counters with numerical indicator tubes that are simpler and less expensive than the usual designs based on bistable multivibrators (flip-flops). This is clearly shown by Fig. 5, giving the circuit diagram of one decade of such a counter. The component values have been so chosen that no stringent requirements are imposed on the amplitude and duration of the input pulses or the constancy of the supply voltages.

To explain the operation of this circuit the SCS denoted by S_0 will be assumed to be in the ON state, the cathode 0 of the indicator tube being lit. The anode and collector of S_0 are then at a low potential (about +1 V and +0.2 V respectively), whereas the collectors of the other SCS's have potentials that may range from +15 V to +120 V, depending on the probe currents of the relevant cathodes of the indicator tube and the leakage currents of the SCS's.

If, now, a negative-going pulse of about 12 V is fed to the input, the anode voltage of S_0 (and obviously also that of the other even numbered SCS's) will momentarily drop to about −5 V. As a result, S_0 is switched off, and after about 2 µs (the turn-off time of the SCS) the current of the indicator tube is thus prevented from flowing through S_0. This current will therefore flow via C_{10} into the base of S_1 so that the latter is switched on.

The collector voltage of S_0 at first increases suddenly owing to the voltage drop across R_{10}, then rises exponentially towards a value equal to the difference between the supply voltage of the indicator tube and its maintaining voltage. Once cathode 1 of the indicator tube has taken over the glow discharge from cathode 0, the collector potential of S_0 continues to rise, but at a much lower rate, to a potential dictated by the probe characteristic of cathode 0. (It should be kept in mind that the base-emitter diode of S_1 maintains the lower end of capacitor C_{10} almost at earth potential.)

Although the input pulse also reduces the anode voltage of the odd numbered SCS's, this does not prevent S_1 from being switched on; the circuit has been so dimensioned that the anodes do not at first drop below about +6 V.

Once S_1 is switched on, its collector potential drops to about +0.2 V and its anode potential to about +1 V, as does the anode potential of the other interconnected, odd numbered SCS's; the anode potential of the even numbered SCS's, however, rises to +12 V. The collectors of all SCS's, except the one that is switched on, again assume high positive potentials, governed by the probe characteristics of the several cathodes of the numerical indicator tube. The next pulse will therefore switch S_1 off and S_2 on, and so forth. Connection of the odd and even numbered anodes to alternate lines thus ensures that — even with fairly wide tolerances on the duration of the input pulse — the correct SCS will always be switched on.

At the tenth pulse S_9 is switched off and S_0 is switched on again. As a result, the voltage of cathode 0 drops rapidly to about +0.2 V. The potential of the carry output terminal, which is normally +12 V owing to the presence of clamping diode D_1, then also drops to about +1 V. A well-defined carry output signal is thus provided which can advance a following, identical decade counter one step.

The supply voltage V_{BB} of the numerical indicator tube should be 180 V +5%; the required supply voltage V_{CC} for the SCS's is 12 V±15%. Provided the various components are given the values quoted in the caption of Fig. 5, the amplitude of the negative-going input pulses is allowed to range from $0.75V_{CC}$ to $1.25V_{CC}$; their duration and interval should be at least 5 µs and 20 µs respectively. (A convenient pulse shaper is described in the following section.)

To clear the memory and darken the indicator tube, the common emitter line of the SCS's is momentarily interrupted by means of switch *Sw*, so that its potential rises to about +4 V and any previously switched-on SCS becomes non-conducting.

To start the ring counter, cathode 0 of the darkened indicator tube can be lit by feeding a single positive-going pulse to the reset terminal. A circuit for originating a suitable pulse with the aid of a push button switch is described on p. 6.

Pulse Shaper

Fig. 6 shows the circuit of a pulse shaper suitable for supplying input signals to the ring counter described above. A positive-going pulse fed to the base of the BRY39 gives rise to a substantially square-wave pulse of fixed amplitude and duration at the collector.

In the quiescent condition the base is biased to the emitter potential, 0 V, and the SCS is switched off. In response to a positive-going pulse fed to the base via capacitor C_1, the initial bias is temporarily overcome and the SCS is switched on, anode current being supplied via capacitor C_2. Since the current flow through resistor R_1 is insufficient to maintain the SCS in the switched-on condition, the period of conduction depends on the charging time of C_2. As the charge increases the anode current decreases, eventually falling off to a value at which conduction can no longer be maintained in the SCS; at this point, therefore, the SCS switches off and the capacitor C_2 discharges via R_1.

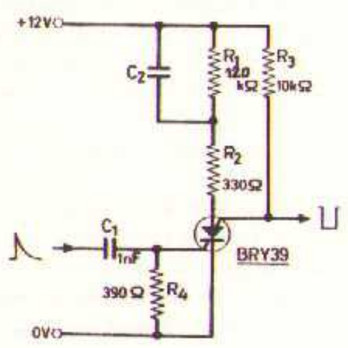


Fig. 6. Pulse shaper for driving the ring counter of Fig. 5.

The desired output signal is taken from the collector, at which a negative-going pulse of almost constant amplitude, equal to the supply voltage minus about 0.2 V, appears; its duration is equal to the period of conduction of the SCS, which is governed by the time constant R_2C_2 and to some extent by the holding current of the individual SCS. The larger the time constant, the longer the pulse duration and the lower the maximum repetition frequency will be.

Reset Pulse Generator

The circuit of Fig. 7 supplies a suitable pulse for resetting the previously described ring counter to zero after its indicator tube has been darkened. An important feature of this circuit is that, once the switch has been closed, spurious impulses due to contact bounce have no effect; a single output pulse of fixed shape is produced, with which all decades of the counter can be reset simultaneously.

Upon closure of switch *Sw*, as soon as capacitor *C* is charged, the SCS is switched on by the current flowing into its base. The capacitor then rapidly discharges via the SCS and its emitter resistor R_4, across which a positive-going reset pulse of the required duration is produced. This pulse subsequently decays to a very low value determined by the ratio of R_3 and R_4 and ceases completely when the switch is released.

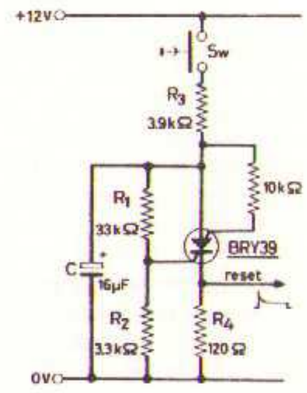


Fig. 7. Circuit producing a pulse for simultaneously resetting a number of darkened decade ring counters to zero.

Ring Counter without Numerical Indicator Tube

In some cases a decade counter is required which need not display the number of pulses on a numerical indicator tube. Such a counter may, for example, be used for driving a control circuit for a numerical print-out device (see p. 8). In that case the circuit of Fig. 5 may be simplified as indicated in Fig. 8.

Comparison with Fig. 5 shows that the indicator tube has been replaced by ten resistors (R_{10} to R_{19}) linked to a common supply line. To ensure that the collectors of the SCS's remain positive with respect to their anodes, even in the event of a heavy external load, this line should be connected to a +24 V source; if the +12 V line were used, an SCS might be wrongly switched on via its internal "p-n-p transistor".

Negative-going pulses can be taken from the terminal points 0, 1, 2, . . . , 8 and 9. To limit the amplitude at any of the terminal points to about 11 V, a combination of a clamping diode and a 10 kΩ resistor may be connected between the relevant terminal point and the +12 V supply line; the output pulse should then be taken from the junction of the diode and its resistor (cf "carry output" in the circuit of Fig. 5).

The voltage dividers formed by R_{10}, R_{20} and R_{30}, and by R_{11}, R_{21} and R_{31} and so forth have been so dimensioned that high pulses appearing on the +24 V supply line when one SCS is switched on will not interfere with any other SCS.

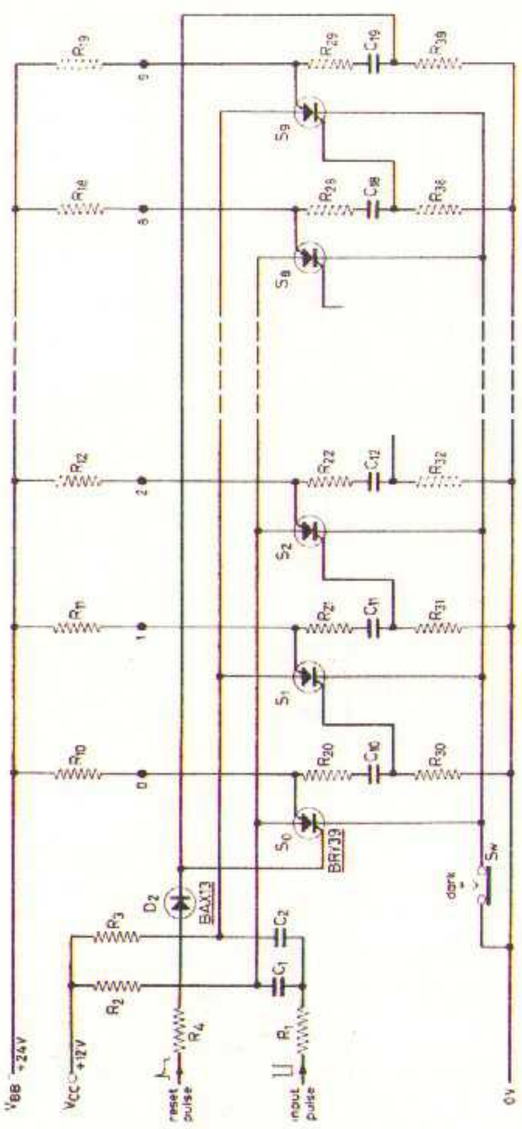


Fig. 8. Ring counter without numerical indicator tube.

R_1	820 Ω
R_2	4.3 kΩ
R_3	4.3 kΩ
R_4	2.2 kΩ
R_{10}-R_{19}	2.2 kΩ
R_{20}-R_{29}	3.9 kΩ
R_{30}-R_{39}	1 kΩ
C_1, C_2	5.6 nF
C_{10}-C_{19}	1 nF

Pulse Gate Circuits

The BRY39 lends itself particularly well to use in synchronous gating; that is, in carrying out switching and logic functions that are to be coordinated by a train of clock pulses. A synchronous gate reponds only when a clock pulse is presented to it concurrently with the required levels at its input terminals. The shape of the output pulse need not depend on that of the input (which may be degraded), as is usually the case in non-synchronous gates; with the aid of the clock pulse, output pulses of well-defined, uniform amplitude and duration can be obtained.

In the gate circuits to be described, input pulses are applied to the collector and clock pulses to the emitter of the SCS, output pulses being taken from the anode. Thus negative-going pulses of about 12V, supplied for example by the previously discussed ring counters, afford a suitable input (without needing to be inverted), and the output of the gate is itself suitable for driving such a counter.

Simple AND Gate

The operation of the simple gate circuit shown in Fig. 9 may be explained as follows. Negative-going clock pulses reducing the relevant line voltage from ±12 V to zero are applied to terminal *1*. If, during the presence of such a clock pulse, a negative-going input signal is fed to terminal *2*, all conditions are fulfilled for switching on the SCS. The resulting anode current flowing through R_2 lowers the potential of terminal *3* giving rise to a negative-going square-wave output pulse that persists until the end of the clock pulse.

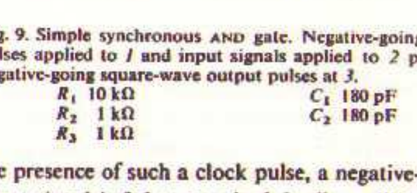


Fig. 9. Simple synchronous AND gate. Negative-going clock pulses applied to *1* and input signals applied to *2* produce negative-going square-wave output pulses at *3*.

R_1	10 kΩ	C_1	180 pF
R_2	1 kΩ	C_2	180 pF
R_3	1 kΩ		

Capacitor C_2 limits the feedback introduced by the anode resistor R_2.

AND Gate with Additional Delayed OR Input

The gate circuit shown in Fig. 10 is provided with an additional OR input and incorporates a delay network. If a zero level is applied to *any* of the diodes D_1, D_2 or D_3, a potential of about 6 V appears at the upper end of capacitor C_2, so that diode D_4 is reverse-biased and has no effect. The operation of the circuit is then identical to that of Fig. 9, and provided a clock pulse is applied to input *1*, an input pulse fed to terminal *2* will result in an output pulse.

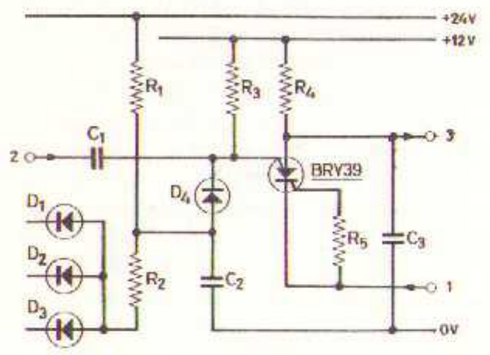


Fig. 10. AND gate similar to that of Fig. 9, but with additional delayed OR input.

R_1	22 kΩ	R_5	1 kΩ
R_2	6.8 kΩ	C_1	180 pF
R_3	10 kΩ	C_2	1 nF
R_4	1 kΩ	C_3	180 pF

If, on the other hand, a positive d.c. level of 12 V is applied to all diodes D_1, D_2 and D_3, diode D_4 will be forward biased. A negative-going input pulse applied to terminal *2* will therefore be passed by this diode and absorbed by capacitor C_2, so that it no longer has any effect.

The network R_2C_2 introduces a delay to ensure that a change of the d.c. level has no effect until the following clock pulse has appeared.

AND Gate with Additional Delayed AND Input

In the circuit of Fig. 11, which is similar to that of Fig. 10, the diodes D_1, D_2 and D_3 are reversed so that the d.c. input forms an AND function. Input pulses fed to terminal *2* will have effect only if *all* d.c. inputs have zero potential and no input is at a potential of +12 V or more.

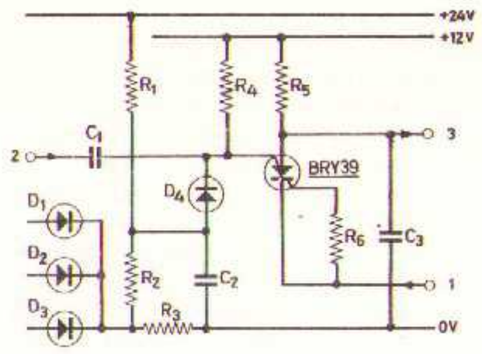


Fig. 11. AND gate similar to that of Fig. 9, but with additional delayed AND input.

R_1	22 kΩ	R_4	10 kΩ	C_1	180 pF
R_2	6.8 kΩ	R_5	1 kΩ	C_2	1 nF
R_3	10 kΩ	R_6	1 kΩ	C_3	180 pF

Control Circuit for Numerical Print-out Devices

Fig. 12 shows a circuit designed for driving a numerical print-out device. Apart from the "add" and "non-add" stages, only the first and the last of the ten stages for energising the coils 0 to 9 of the print-out device are shown. (For printing-out the complementary digits, as frequently required, the stages 0 to 9 should obviously be connected to the coils 9 to 0 respectively.)

The operation of the circuit resembles that of a monostable multivibrator, with S_1, which is normally switched on, governing the period. If one of the SCS's designated S_{10} to S_{21} is switched *on*, a negative-going pulse due to the fall of its anode potential from +12 V to about +1 V is passed, via C_2 and C_1, to the anode of S_1, causing the latter to be switched *off*. Following its initial drop, however, the anode potential of S_1 rises towards +24 V at a rate governed by R_2 and $C_{1,2}$; after a short interval it exceeds the collector potential of +12 V and S_1 becomes conducting again. The negative-going pulse due to the resulting drop in anode potential is then passed, via C_1 and C_2, to the common anode line of S_{10} to S_{21} and causes the SCS, which started the cycle, to be switched off.

The input circuits for the stages governing coils 0 to 9 are similar to those of the gate circuits discussed earlier. Negative-going clock pules (or pulses which are derived from and synchronous with them) are fed to their common input terminal. As long as the level of the d.c. input terminal exceeds +12 V the corresponding diode (D_{10} to D_{19}) will be conducting so that these clock pulses have no effect. However, after the d.c. input voltage is made to drop to about zero (1-level) and the corresponding capacitor (e.g. C_{20}) is discharged, the diode becomes non-conducting. Owing to the incorporated delay the required SCS is not switched on until the next clock pulse occurs.

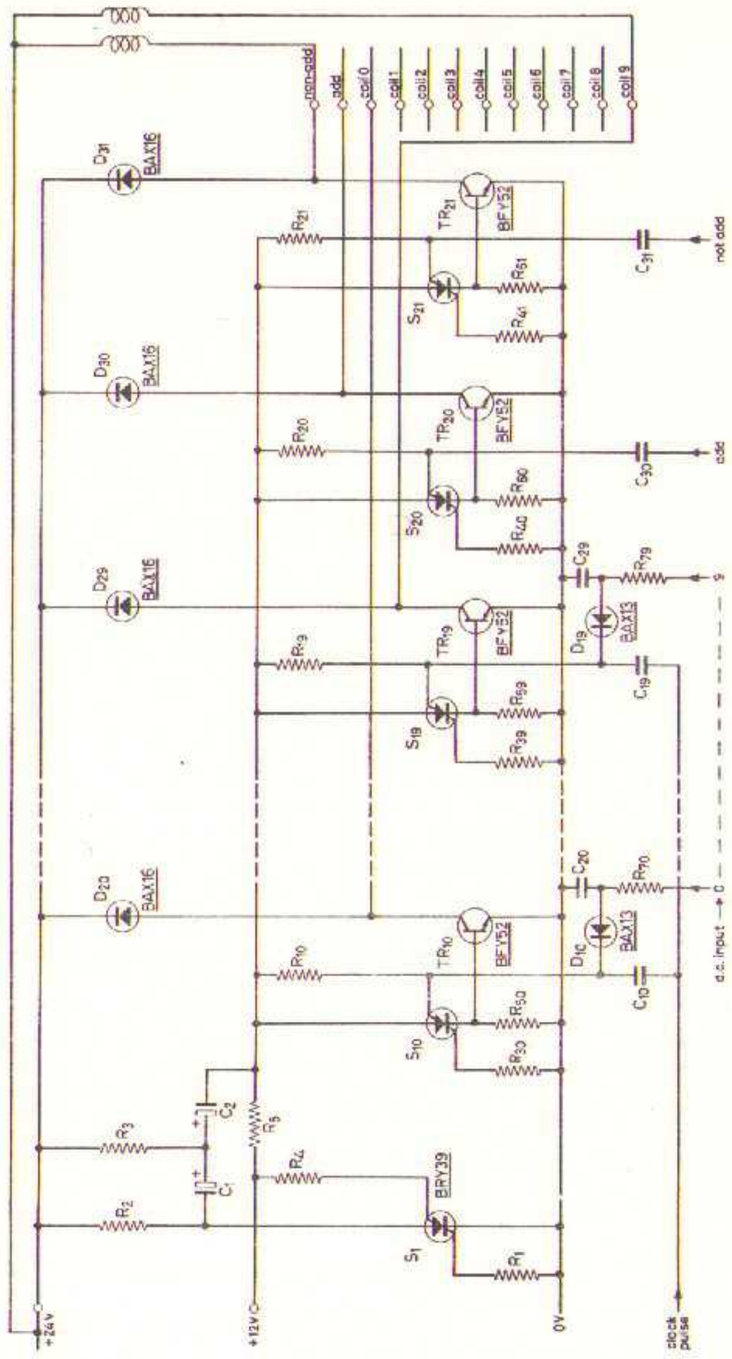


Fig. 12. Control circuit for numerical print-out devices.

R_1	5.6 kΩ	R_{50}-R_{61}	1 kΩ
R_2	3.9 kΩ	R_{70}-R_{79}	10 kΩ
R_3	100 kΩ	C_1	10 µF, 25 V
R_4	1 kΩ	C_2	10 µF, 25 V
R_5	390 Ω	C_{10}-C_{19}	180 pF
R_{10}-R_{21}	1 kΩ	C_{20}-C_{29}	1 nF
R_{30}-R_{41}	1 kΩ	C_{30}-C_{31}	180 pF

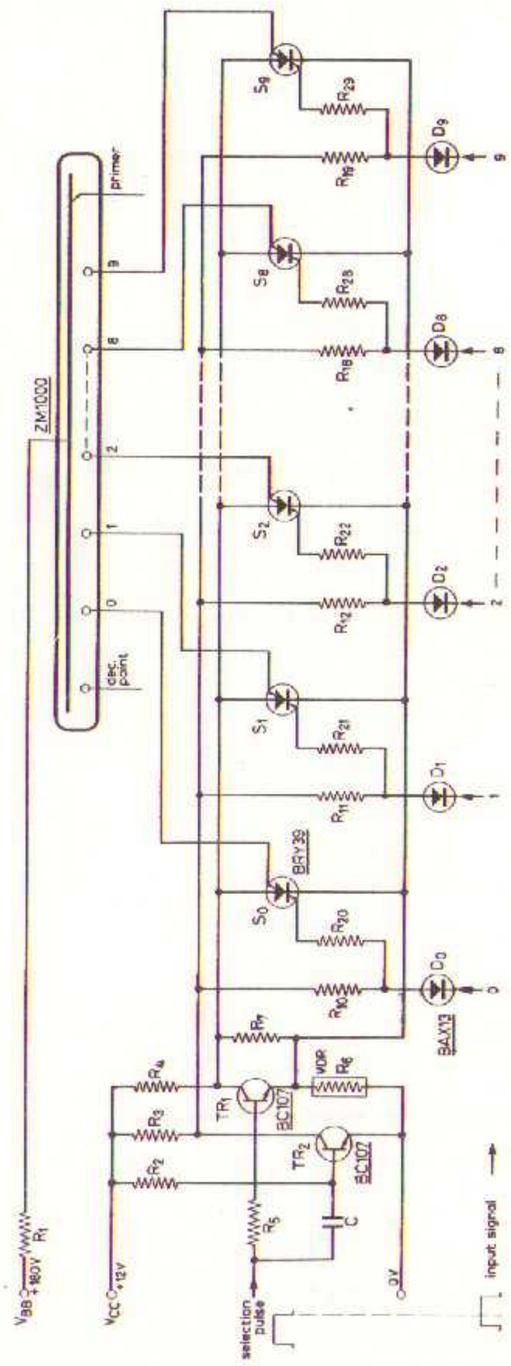
The last two stages of the circuit can control the "add" and "non-add" coils of the print-out device. After the number to be recorded has been printed out in its entirety, a negative-going pulse fed to the corresponding terminal will directly switch on the SCS marked S_{20} or S_{21} so that the "add" or "non-add" coil of the printer is energised.

The diodes D_{20} to D_{31} safeguard the transistors against voltage surges that are apt to be produced across the energising coils when they are switched off.

The circuit can produce energising pulses of up to about 300 mA with a duration of 35 ms, as required for the less sophisticated types of print-out devices. If a faster print-out device is used, requiring energising pulses with a duration of only 1 ms, the transistors (TR_{10} to TR_{21}) can be dispensed with and the coils may be taken up directly in the anode circuits of the SCS's. And if the energising current required is also smaller (for example 100 mA), the circuit can be further simplified by incorporating the coils directly in the collector circuits of the SCS's. In both cases, of course, other appropriate changes must be made in the control circuit.

Numerical Display Unit with Memory

Parallel digits, representing information from a computer or calculator, are often displayed on a bank of numerical indicator tubes (such as the ZM1000), each tube presenting the digit of one decade. A circuit for controlling one such tube in an output display bank is shown in Fig. 13. The SCS associated with each digit acts as a switch and a memory, the digit displayed remaining lit after the information pulse (input signal) that selected it has ceased. The operation of the circuit will be explained with reference to a display bank in which indicator tubes are energised in sequence until the entire numeral to be indicated is on display.



The indicator tube to be energised is first selected by applying a positive-going pulse to the selection pulse input of the control circuit associated with it. This bottoms transistor TR_1 in the circuit of that tube and drives the anode-emitter voltage of all its associated SCS's to so low a value that none of them can remain conducting; any previously displayed digit is therefore extinguished and the memory is cleared. At the end of the selection pulse TR_1 returns to the cut-off condition and the potential of the common anode line rises; at the same time, the trailing edge of the selection pulse temporarily cuts off TR_2 and now the common base line also rises, towards +12 V. If a positive-going pulse is now present at one of the input signal terminals, causing the diode at that terminal to be reverse-biased, current flows into the base of the associated SCS so that it is switched on and the required cathode of the numerical indicator tube is lit. Because of the previously described holding action of the SCS, it continues to conduct and the cathode remains lit after the initial input signal has ended.

To ensure that only the required digit is switched on, all diodes must normally be forward biased during the presence of a selection pulse; except where the bias is momentarily reversed by a positive-going input signal, the currents through resistors R_{10} to R_{19} will then flow through the diodes instead of into the bases of the SCS's associated with them.

The trailing edge of the selection pulse keeps TR_2 cut off only for a short interval determined by the time constant R_2C. As soon as it is again bottomed, the common base line returns to a low potential and the voltage drop across the voltage dependent resistor R_6 positively biases the emitters of the SCS's. Any digit input pulse that arrives after the end of the circuit selection pulse therefore has no effect; it cannot cause an SCS to be switched or the indicator tube to change its indication.

This makes it possible to connect similar digit input leads of all indicator tubes in the display bank in common; a digit input pulse applied to the commoned leads will be registered only by that indicator tube the control circuit of which has also received a selection pulse. Moreover, the source of the digit input signal is not called upon to supply current to the circuit; on the contrary, the direction of current flow is normally from the control circuit to the signal source (opposite to the direction of the arrows in Fig. 13), and at the terminal to which an input signal is applied it is no more than a very small leakage current. This makes it possible for one low-power transistor to drive a considerable number of commonly connected input terminals if required.

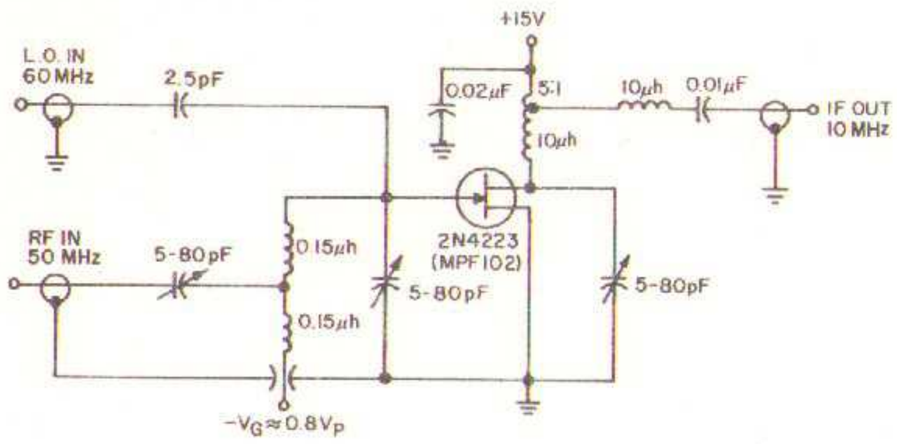
The primer of the ZM1000 indicator tube need not be used, nor do the probe currents of the unlit cathodes affect the operation of the circuit. Owing to the emitters of the SCS's being positively biased by R_6, the probe currents are conducted via the collector, the base and the base resistors of each SCS and thence via the bottomed transistor TR_2 to earth without causing the base-emitter junction of any SCS to become forward biased. In this way the collector voltages are prevented from oscillating.

To darken the indicator tube, it is sufficient to apply a positive-going pulse to the selection pulse input while all digit inputs are at their (normal) low potential; this will switch off any conducting SCS and extinguish the indicator tube cathode associated with it.

The 180 V supply V_{BB} and the 12 V supply V_{CC} should be constant within ±5%. The high level of both the selection pulse and the digit input signal may range from +4 V to ±25 V; the recommended value is +6 V. The low level may range from −1 V to +0.2 V, zero being recommended. The duration of the selection pulse should not be less than 6 µs and that of the digit input signal not less than 5 µs; the input signal should be applied before the end of the selection pulse.

Fig. 13. Numeric l display unit with memory (optimum design for V_{BB} = 180 V ±5% and V_{CC} = 12 V ±5%).

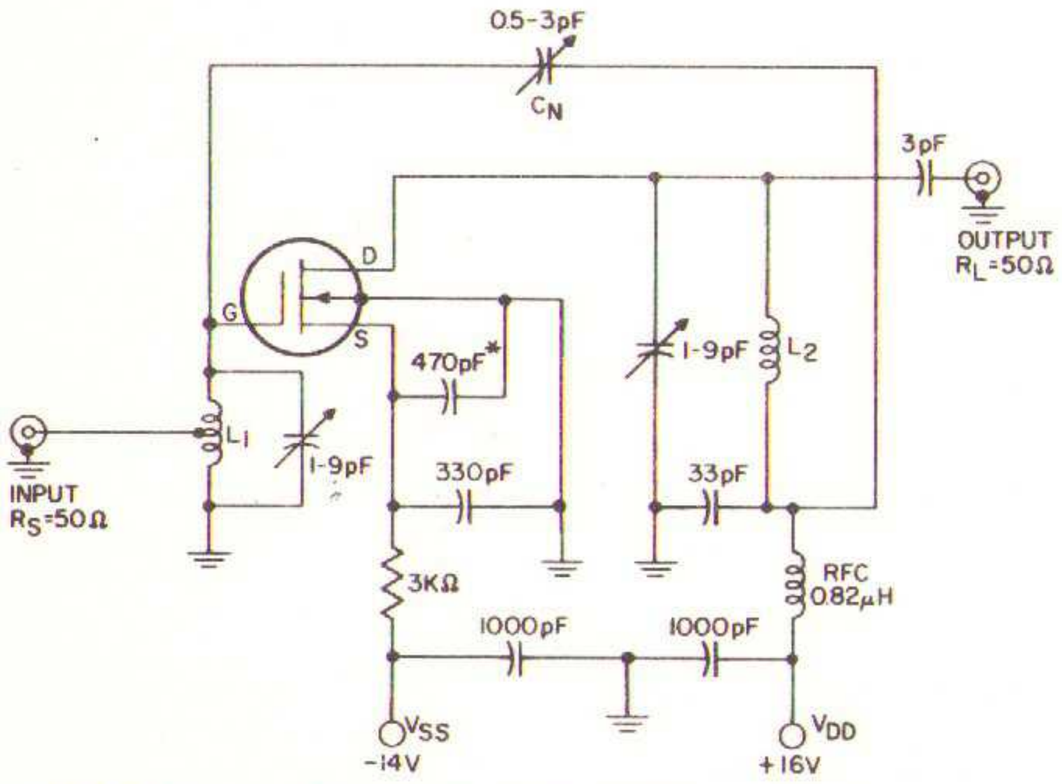
R_1	16 kΩ ±3%	R_6	Type 2322 574 90002
R_2	10 kΩ ±5%	R_7	8.2 kΩ ±5%
R_3	1.2 kΩ ±5%	R_{10}-R_{19}	8.2 kΩ ±5%
R_4	2.2 kΩ ±5%	R_{20}-R_{29}	3.3 kΩ ±5%
R_5	2.2 kΩ ±5%	C	2.7 nF ±10%



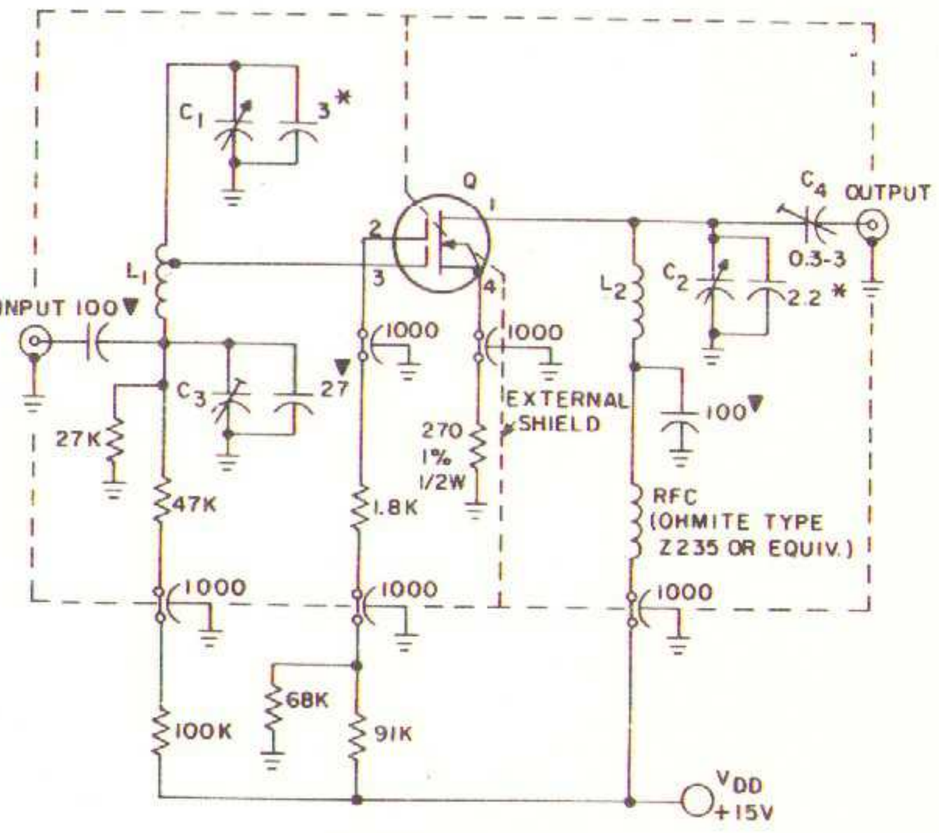
Using FETs To Improve Mixer Circuit Performance

By biasing the gate-to-source voltage of an 2N4223 (MPF102) field effect transistor, at 80% of its pinch-off voltage — V_{GS} = 0.8 V_P, mixer circuits can be developed which yield an excellent balance of performance characteristics such as shown below:

Conversion Gain	16 dB
Noise Figure	5.5 dB
Image Rejection	12 dB
Cross Modulation — 50 mV (Undesired)	



200-MHz Common-Source Neutralized RF amplifier utilizing Type 3N128
Q = Type 3N128



* TUBULAR CERAMIC
▼ DISC CERAMIC

200-MHz RF Amplifier utilizing Type 3N140
Q = Type 3N140

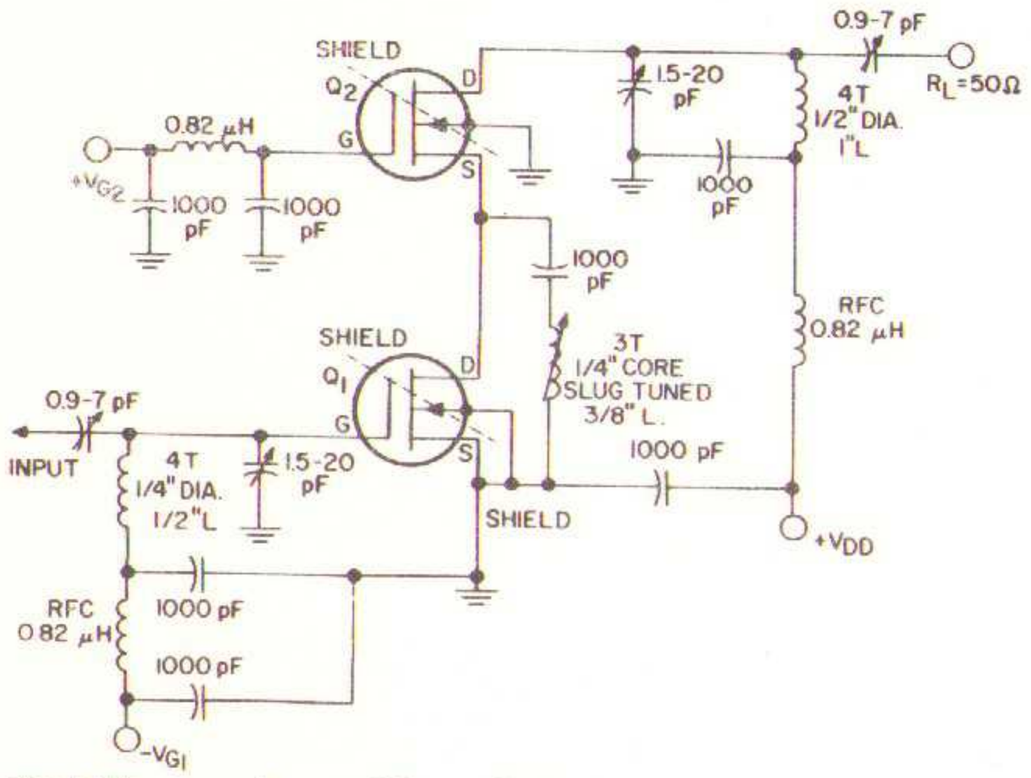
C_1, C_2: 1.5-5 pF variable air capacitor: E. F. Johnson Type 160-102 or equivalent

C_3: 1-10 pF piston-type variable air capacitor: JFD Type VAM-010, Johanson Type 4335, or equivalent

C_4: 0.3-3 pF piston-type variable air capacitor: Roanwell Type MH-13 or equivalent

L_1: 5 turns silver-plated 0.02″ thick, 0.07″-0.08″ wide copper ribbon. Internal diameter of winding = 0.25″; winding length approx. 0.65″. Tapped at 1½ turns from C_1 end of winding

L_2: Same as L_1 except winding length approx. 0.7″; no tap.



200-MHz cascode amplifier utilizing Type 3N128
Q_1 and Q_2 = Type 3N128

400-MHz RF Amplifier utilizing RCA Developmental Type TA7153
Q = RCA Dev. No. TA7153

L = 1″ Length, 3/16″-Dia. Brass or Copper Rod, Silver Plated.